THROUGH-PACKAGE-VIA HOLE FORMATION, METALLIZATION AND CHARACTERIZATION FOR ULTRA-THIN 3D GLASS INTERPOSER PACKAGES

A Dissertation
Presented to
The Academic Faculty

by

Vijay Sukumaran

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2014

THROUGH-PACKAGE-VIA HOLE FORMATION, METALLIZATION AND CHARACTERIZATION FOR ULTRA-THIN 3D GLASS INTERPOSER PACKAGES

Approved by:

Dr. Rao R. Tummala, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Suresh Sitaraman
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Oliver Brand
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Venky Sundaram
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Muhannad Bakir
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: 1st May, 2014.

To my Grandparents (Ammi & Athimber) and Parents (Amma & Appa)

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my advisor Professor Rao R Tummala for giving me an opportunity to work on leading edge Glass Interposer research at the Georgia Tech 3D systems packaging research center (GT-PRC). He has always been a great source of inspiration, and his vision and advice have greatly helped shape my thesis. Next, I would like to thank my mentor, Dr. Venky Sundaram, for his constant support and guidance throughout my PhD research.

I would like to express my sincere thanks to my committee members: Professor Oliver Brand, Professor Suresh Sitaraman and Professor Muhannad Bakir for being part of my PhD committee and for all the valuable discussions and feedback.

I feel fortunate to have had the opportunity to work with a very knowledgeable, enthusiastic and helpful research team at PRC and I sincerely thank Dr. Raj Pulugurtha, Dr. Himani Sharma, Dr. Fuhan Liu, Mr. Sung Jin Kim, Mr. Nitesh Kumbhat, Mr. Hunter Chan, Dr. Sunghwan Min (Dr. Max Min) and Dr. Vanessa Smet for all the valuable technical discussions, guidance and help during the course of my study. I would like to thank the administrative staff at PRC: Karen May, Patricia Allen, Brian Mcglade, Traci Walden Monroe, Dean Sutter, Jason Bishop and Chris White for all the help and support during my stay at PRC.

Working at PRC gave me a unique opportunity to interact with industry mentors and visiting engineers from various companies. I would like to thank the member companies of the Silicon and Glass Interposer (SiGI), as well as the Low cost Glass Interposers and Packages (LGIP) consortiums at GT-PRC. The technical guidance and support that I received related to tools, materials or processes has been extremely valuable to my research, and I am grateful for their support. Working with

visiting engineers has been a great learning experience and I am thankful for their friendship. Special thanks to my friends: Yoichiro (Asahi Glass Company, Japan), Yuya (Zeon Corporation, Japan), Makoto and Kodai (Namics, Japan), Toshi and Yutaka (NTK, Japan), Akira (Atotech, Japan), Taiji (Fujitsu, Japan), and Furuya (Ushio, Japan).

My stay in Atlanta has been a joyful experience thanks to my friends: Gokul, Srikrishna, Uppili, Jayaram, Shyam, Debesh, Satyan, Ahmad, Akansha, Rohit, Advait, Swarrnna Karthik, Kiran, Ashok, Sourabh, Ameya, Kanika, Abhishek, Koushik, Dibyajat, Jialing, Yushu, Nithya, Tapo, Qiao, Bruce, Brett, Xian, Zihan, Nathan, Timothy, Saumya, Partha, Kaya, Gary, Sadia, Chandra and Chinmay. Also, the technical help and support from all the interns at PRC is highly appreciated, and I would like to acknowledge their hard work and sincere efforts.

Special thanks to Srikrishna, Gokul, Yoichiro, Koushik, Timothy, Richard Shafer, Bruce and Saumya for the useful discussion and for helping with modeling, fabrication, SEM imaging and characterization.

Table of Contents

LIST OF TABLES

Page

LIST OF FIGURES

Page

SUMMARY

There is an increasing demand for higher bandwidth (BW) between logic and memory ICs for future smart mobile systems. Such high BW are proposed to be achieved using 3D interposers that have ultra-small through-package-via (TPVs) interconnections to connect the logic device on one side of the interposer to the memory on the other side. The current approach is primarily based on organic or silicon interposers. However, organic interposers face several challenges due to their poor dimensional stability, and coefficient of thermal expansion (CTE) mismatch to silicon ICs. Silicon interposers made with back-end-of-line (BEOL) wafer processes can achieve the required wiring and I/O density, but are not cost effective, and in addition exhibit higher electrical loss due to the semiconducting nature of the Si substrate. In this research, ultra-thin 3D Glass Interposers are studied as a superior alternative to organic and silicon interposers. The fundamental focus of this research is to achieve ultra-small TPVs in thin glass with dimensions similar to that of through-silicon-vias (TSVs) in silicon.

The objective of this research is to study and demonstrate ultra-small pitch (30µm) TPV hole formation (10µm diameter), metallization and electrical characterization in ultra-thin (30µm) glass substrates. To meet these objectives, this study focusses on four main research tasks: a) electrical modeling and design of ultra-small TPVs in glass, b) small diameter TPV hole formation with minimum defects, c) copper metallization of TPVs with reliable adhesion, and d) electrical characterization of TPVs.

This research reports the first demonstration of ultra-small TPVs (10-15µm in diameter) in ultra-thin glass interposer substrates (30µm). A thin-glass handling method is developed using polymer surface layers to achieve defect-free handling of

glass even at thicknesses as low as 30µm. Several TPV formation methods are explored including excimer laser ablation using 193nm (ArF) lasers to form TPVs with smallest diameter and pitch. A brief study on the through-put capabilities of these excimer lasers is also discussed. The fundamental approach to TPV metallization involves a semi-additive-plating process (SAP) using electroless and electrolytic copper deposition techniques. The resulting side-wall surfaces of TPVs after metallization are analyzed through SEM imaging of TPV cross-sections, and are further characterized using nano-indentation tests. Additionally, thermo-mechanical reliability tests and failure analysis are performed to study the reliability of TPVs that are metallized with Cu. This research culminates in design, fabrication and electrical characterization of small pitch TPVs in ultra-thin glass interposers (30µm).

The intellectual contribution and novelty of this dissertation can be summarized as follows:

- First exploration of 3D Glass Interposer Package concept, with ultra-small TPVs in glass at same dimensions like TSVs.
- Concept of Ultra-thin (30µm) glass substrates with new polymer dielectrics for improved handling, defect-free TPV formation and ease of copper metallization.
- Investigation of methods for defect-free formation of small TPVs (10-15µm diameter) at small pitch (< 30µm) through laser-glass interaction studies and surface morphology analysis.
- Panel-based double-side fabrication approach to achieve the thinnest glass interposer substrate reported till date.
- Ultra-miniaturized and SMT compatible RF filter integration in double-side glass interposers with small pitch TPVs.

Chapter 1

INTRODUCTION

The recent evolution of portable electronic systems such as smartphones began to drive advanced packaging technologies with the following attributes: a) high performance, b) small form-factor, c) low cost, and d) high functionality. Transistor scaling has enabled miniaturization at the device level through the implementation of the system-on-chip (SOC) approach, but even so, there are fundamental challenges with achieving all smartphone system functions in a single chip. These challenges are due to: a) processing requirements at different technology nodes for disparate functional blocks (RF, digital, analog, and sensors), b) interference between the disparate functional blocks, c) design complexity and d) cost considerations. Efforts to overcome these challenges have led to many new concepts including separate dies for each function and stacking of these dies with shortest and high band-width routing in-between. At present, two concepts are being developed to achieve high-density routing between separate dies: 3D IC stacks interconnected with through-silicon-vias (TSVs) and 2.5D with side-by-side ICs. A third concept, called 3D interposer, is proposed by Georgia Tech. All of these architectures can be referred to as a short term strategy towards integrating the entire system on a single carrier or substrate (system-on-package: SOP) in the long term. The SOP approach provides heterogeneous integration and helps achieve system goals for cost, miniaturization, functionality and performance [1-3]. A schematic cross-section of the SOP approach is shown in Figure 1.

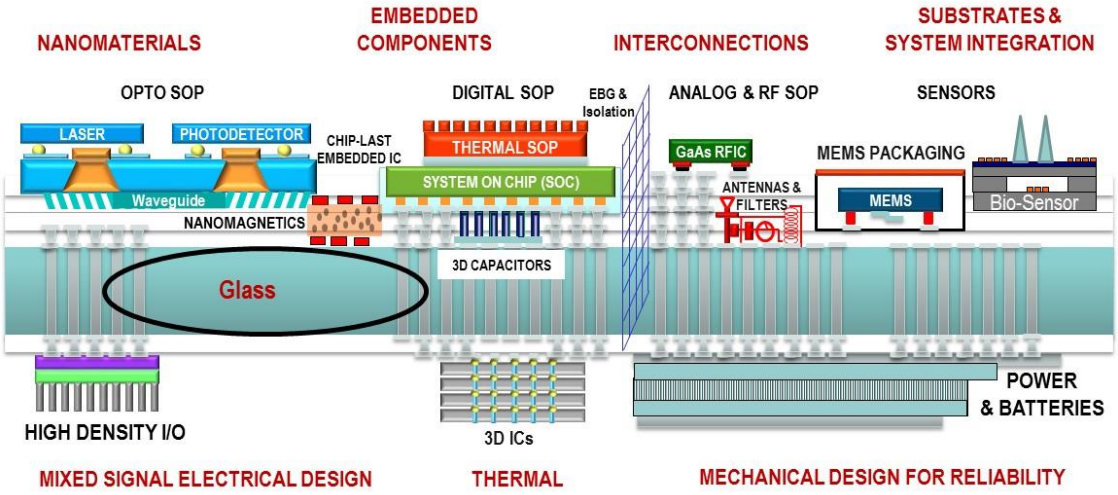


Figure 1: System Scaling with 3D SOP concept requiring Small pitch TPVs in ultra-thin glass interposers-by Prof. Rao Tummala (GT-PRC).

As Figure 1 illustrates, in the SOP approach, heterogeneous and system-level functions require 3D and 2.5D package structures that enable ultra-high-density interconnections between ICs; for example, between the logic and memory ICs. Such interconnections are initially achieved with interposers that would then become BGA packages and eventually system packages in the SOP concept.

1.1 Need for 3D Interposers

Improvements in high-bandwidth can be achieved in two ways: a) high speed data processing (in logic) and b) high speed data transfer or communication (high-bandwidth) between memory and logic devices. There has always been an increasing demand for higher and higher bandwidth interconnections between logic and memory ICs. This need is currently being met by package-on-package (POP), which provides the bandwidth in the form-factor required of today's smart systems [4]. Figure 2 illustrates the current and future demand for high-bandwidth between logic and memory ICs in smartphones.

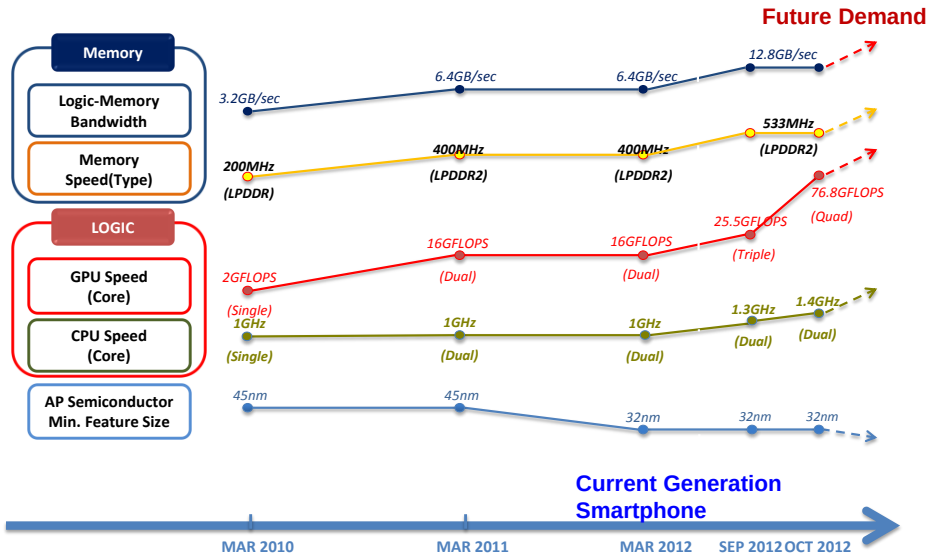


Figure 2: Trend for computational speeds and bandwidth between logic and memory ICs that shows the increasing demand for high bandwidth in future smartphone systems.

3D stacking of ICs using TSVs is being widely developed as the ultimate solution to achieve the highest possible bandwidth enabled by the shortest interconnection length [5-7]. However, such an approach poses several challenges including: a) need for TSVs in the logic die, b) thermal management within the 3D stack, c) high cost of TSV interconnections, and d) manufacturing infrastructure [8, 9]. To overcome these challenges, an approach referred to as 3D interposer was proposed by Georgia Tech, and this approach is being developed as a compelling alternative to 3D ICs with TSVs [10, 11]. Figure 3 illustrates both these approaches. 3D interposers like 3D ICs are able to provide ultra-high density interconnections with ultra-high bit-rate per interconnection. Moreover, a 3D interposer approach eliminates the need for TSVs through logic die (Figure 3b). High density interconnections between the logic and memory ICs in the 3D interposer concept are achieved by using very thin interposers (glass) with small-pitch TPVs having diameters comparable to TSVs within 3D IC stacks. The 3D glass interposer approach thus provides a compelling alternative for achieving high bandwidth by means of: a)

high density TPVs in glass, b) ultra-short interconnection length between logic and memory, and c) ultra-low loss substrate.

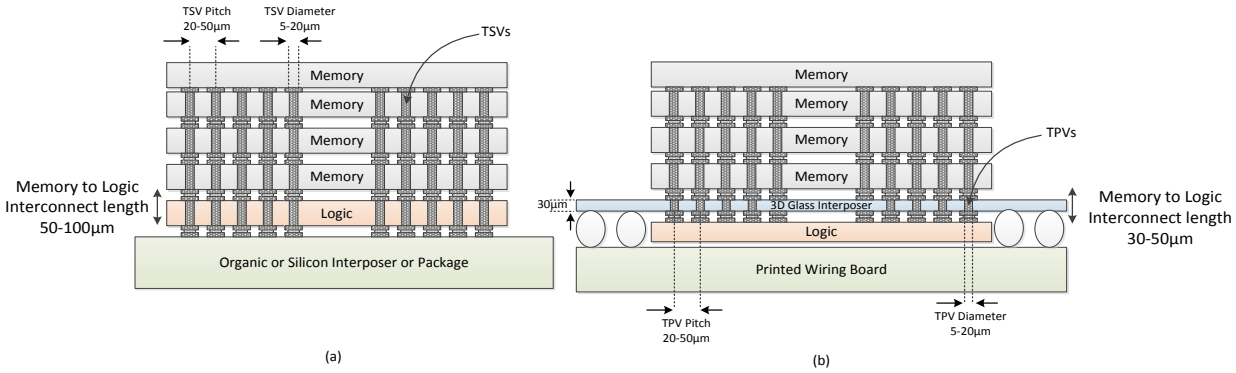


Figure 3: Logic-to-memory interconnections in a) 3D IC stack approach with small pitch and short TSVs and b) 3D interposer approach with small pitch and short TPVs.

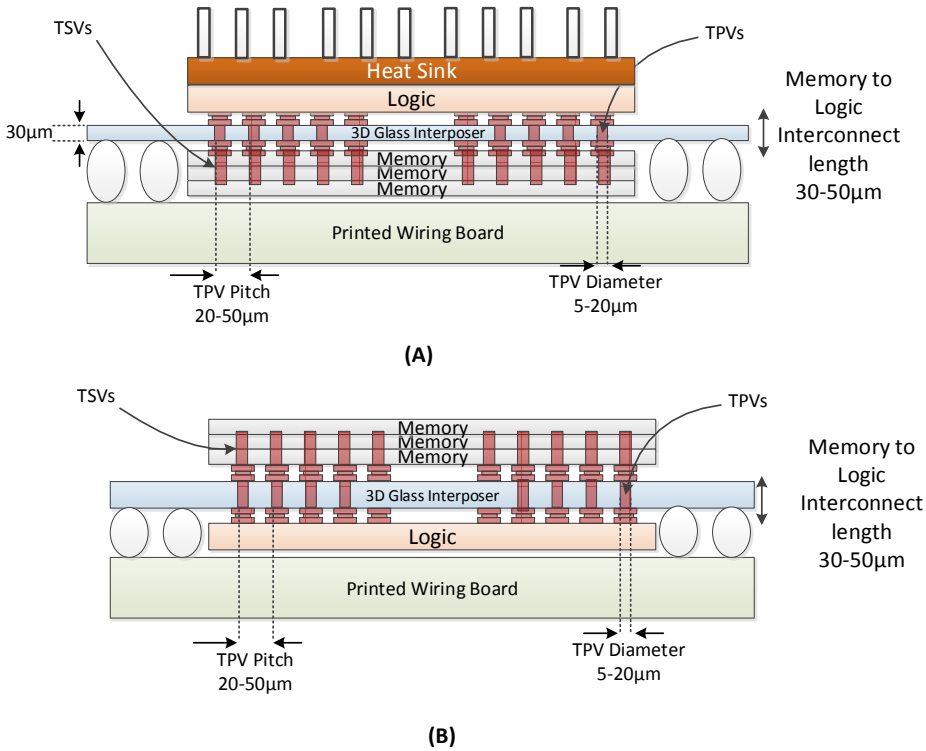


Figure 4: Two different configurations of logic and memory ICs within 3D Interposer approach: A) Logic on top for high power applications and B) Logic at the bottom for low power mobile.

In the 3D interposer approach, when using thermally insulating materials such as glass for interposers, it is important to effectively dissipate the heat from the logic ICs. For high power applications it may be desirable to assemble the logic IC on the top (connected to a heat sink) and the 3D memory stack on the bottom. On the other hand, for low-power mobile applications, the logic could be connected to the bottom side with the memory stack on top. Thus, depending on the operating power levels and design requirements, the position of the logic and memory ICs within the double-side interposer can be modified as illustrated in Figure 4. In summary, two possible configurations can exist: a) logic on top and memory at the bottom – for high performance applications, that require effective thermal management of the logic die through heat sinks, and b) logic at the bottom and memory on top – for low-power mobile applications.

1.2 Interposers versus Packages

a) What is an Interposer?

An interposer is an electronic substrate that provides ultra-high density interconnections between ICs either in 2D or in 3D. The difference between package and interposer is related to the I/O density as measured by I/O pitch at chip level. As shown in Figure 5a, the I/O density of ICs on organic BGA are limited to 120µm pitch, but the need to achieve the bandwidth requires much smaller pitch. Hence, there is a need for interposers that achieve I/O pitch of less than 40µm (Figure 5b). The interposer functions as a space-transformer to bridge the interconnection gap between ICs (< 40µm I/O pitch) and organic packages (~ 120µm pitch). The interposer is assembled on an organic BGA package, which is then assembled on the printed wiring board (400-500µm BGA pitch). The interposer must have ultra-high density of horizontal interconnections comprised of many small-conductor traces

(redistribution layers - RDLs) as well as vertical interconnections called through-package-vias (TPVs). The TPVs along with RDL provide in-plane (2D) as well as out-of-plane (3D) interconnections between multiple ICs.

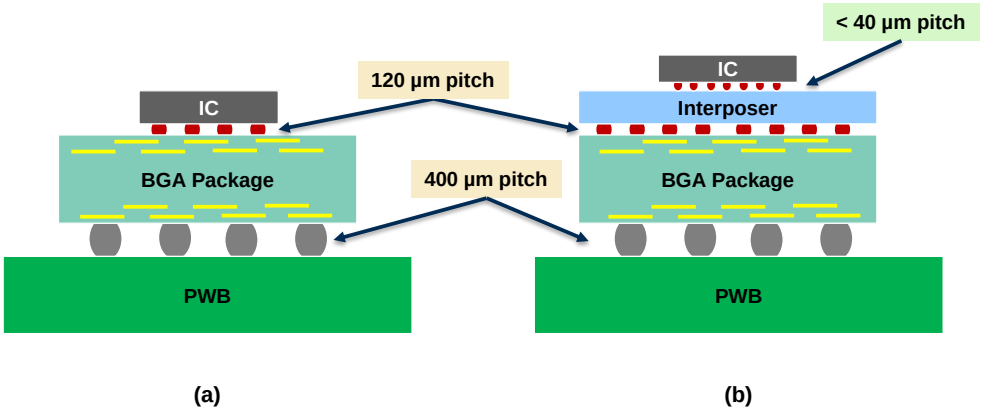


Figure 5: Organic package versus interposer, a) traditional BGA package, b) interposer.

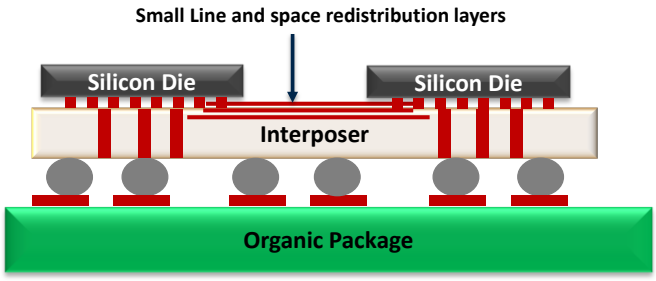
a) Types of interposers

Depending on the way the ICs are interconnected to the interposer, an interposer can be classified into two types:

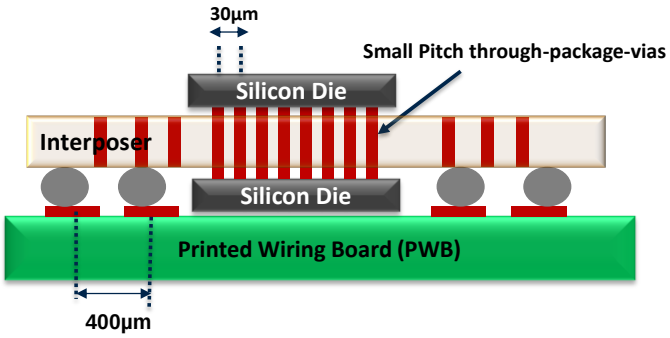
a) 2.5D Interposer

b) 3D Interposer

In a 2.5D interposer, side-by-side integration of ICs or 3D ICs is achieved through RDLs made up of multiple layers of small copper traces interconnected by so called micro-vias. A schematic diagram of a 2.5D interposer is shown in Figure 6a. In fact, such 2.5D silicon interposers have been developed by Xilinx for packaging their FPGA modules [12, 13]. The silicon interposer is fabricated using 65nm/45nm node technology and is subsequently assembled onto an organic BGA package with a BGA pitch of 1mm.



(a)



(b)

Figure 6: Cross-section schematic of Interposers: a) 2.5D side-by-side integration, b) 3D double-side integration.

Although 2.5D interposers achieve high bandwidth interconnections, further improvements in bandwidth are desired with shorter and higher density of interconnections between logic and memory ICs. This can be achieved using 3D interposers with double-side assembly of ICs. A schematic cross-section of a 3D interposer is shown in Figure 6b. Vertical interconnection between ICs on double-side interposers is achieved using small-pitch TPVs as low as 20-40µm in pitch.

1.3 Through-package-via

TPVs provide vertical interconnection between components on double-side 3D interposers. Current interposer technology includes the ability to use organic and silicon substrates. In this research, panel-based 3D glass interposers are studied as a superior alternative to silicon and organic interposers. The evolution of interposer technology is shown in Figure 7. Although TPVs can be formed in organic, silicon or glass substrates, organic and silicon substrates have some limitations.

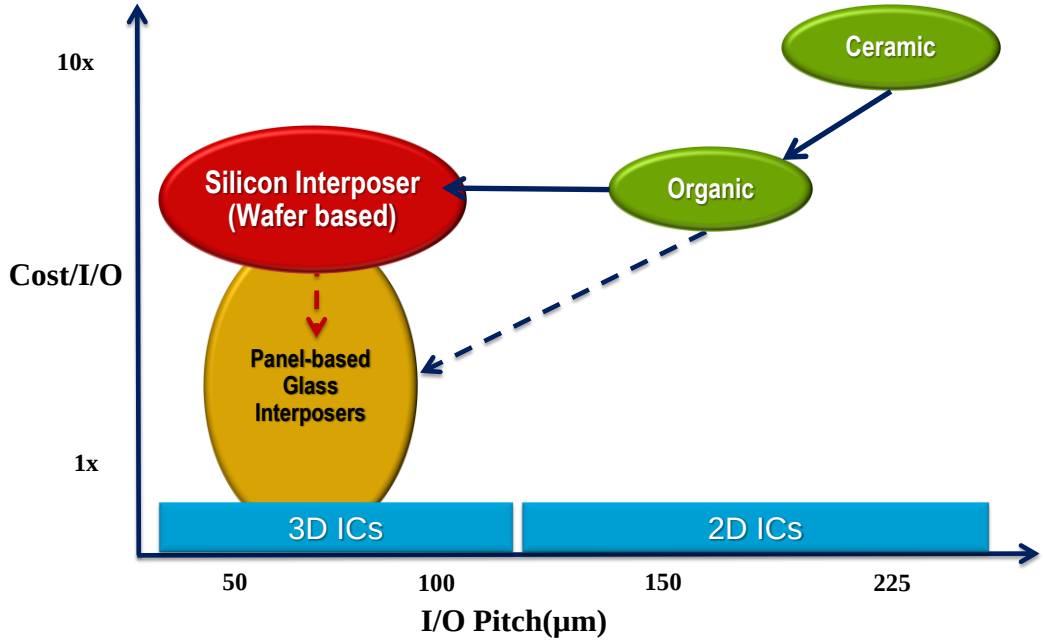


Figure 7: Evolution of Interposer technology as a function of Relative cost and I/O pitch (Prof. Tummala).

The traditional approach to interconnecting individual or multiple ICs is primarily based on using an organic package between the IC and printed circuit board (PCB) [14, 15]. However, there are two major shortcomings with this approach namely: a) difficulty in achieving high I/Os with small bump pitch because of the poor dimensional stability of organic substrates, which requires large capture pads for layer-to-layer via registration, and b) warpage that results from the addition of thinner dielectric layers [16, 17].

Although silicon interposers overcame the challenges of organic packages [18], they pose a different set of challenges such as high cost due to limited wafer size (200-300mm). Limited wafer size yields fewer large interposers per wafer. In addition, the cost of insulating liners for electrical isolation of via conductors is quite high. The high cost is attributed to single-side processes as well as the need for back-grinding and polishing to achieve thin Si interposers. Back-End-of-Line (BEOL) process technologies such as physical vapor deposition (PVD), chemical vapor

deposition (CVD) and Bosch reactive ion etching (RIE) for TSVs are typically used, which also lead to higher costs.

Although organic and silicon interposers pose challenges, each material also has certain benefits. Organic interposers are low in cost due to large panel processing, and silicon interposers help achieve high I/O density due to high thermal stability and surface smoothness. For this study, glass interposers were selected because they offer the benefits of both organic and silicon interposers. Glass interposers allow for large-panel processing and exhibit high thermal stability. In addition, glass has excellent electrical properties. A cross-section schematic of the proposed glass interposer is shown in Figure 8. As shown in Figure 8, interconnections between logic and memory ICs in these 3D double-side interposers are proposed to be achieved using small pitch TPVs in glass. In the future, the glass interposer can be thought of as a BGA package with surface-mountable BGA interconnections.

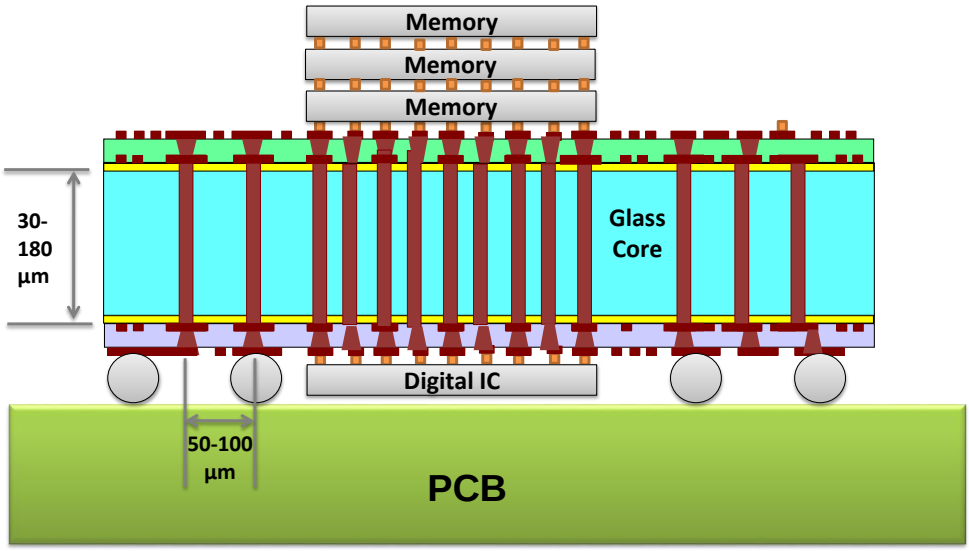


Figure 8: Schematic cross-section of the proposed 3D Glass interposer approach.

1.4 Motivation for Glass Interposers

Glass is proposed by Georgia Tech as the best electronic substrate material due to its favorable material properties [19]. A comparison between the electrical properties, process complexity, and cost associated with glass, silicon, organic and ceramic interposers is listed in Table 1. As shown in Table 1, glass has high electrical resistivity (10^{12} to 10^{16} ohm.cm), resulting in lower insertion loss and cross-talk compared with silicon. In addition, the ultra-smooth glass surface enables direct metallization of conductor traces that have small line-width geometries. Moreover, glass exhibits good dimensional stability, low coefficient of thermal expansion (CTE) similar to silicon die, and high thermal stability. All of these properties suggest that glass would be an outstanding electronic interposer substrate material.

Table 1: Comparison of various alternate materials for interposer application

Material →	**Glass**	**CMOS grade Si (wafer)**	**PV Si (panel)**	**Ceramic**	**Organic**
Electrical Resistivity (ohm.cm)	10^{12} to 10^{16}	$6.4x10^{4}$	$15x10^{-3}$ to $40x10^{-3}$	10^{6}-10^{14}	$> 10^{6}$
Electrical Insertion Loss and Cross-talk	Very low	High	High	Low	Moderate
Ease of via Formation	Slow	Good	Good	Slow	Moderate
Ease of Metallization	Good (direct deposition)	Dielectric liner required	Dielectric liner required	Moderate	Good
Raw Wafer or Panel Cost	Low	High	Low	High	Low
Processed Cost per I/O	Low	High	Moderate	High	High

The specific properties that distinguish glass as an outstanding candidate for substrate material are discussed below:

a) **Electrical properties**: Glass exhibits very high resistivity (10^{12} to 10^{16} Ω.cm) and low loss tangent values (tan δ = 0.002). This insulating behavior of glass allows direct metallization on the glass surfaces, which is not feasible with silicon, that require an oxide liner for electrical isolation between the conductive metal and the semiconducting silicon substrate. Although organic materials also exhibit good electrical isolation, they have a tendency to absorb moisture which degrades their electrical behavior.

b) **Thermal properties**: Glasses are inorganic materials with high rigidity (modulus) and low CTEs. The CTE of glass can be modified by varying the glass composition which includes network formers (inorganic oxides) and network modifiers. This flexibility in CTE is important when considering glass as a package material, especially when the thermo-mechanical stress values need to be optimized for minimum stress at the die-to-interposer and interposer-to-board interconnections simultaneously. The CTE of glass typically can be varied between 0.5 and 10 ppm/^{o}C. Moreover, the high elastic modulus of glass (70-80 GPa) provides excellent rigidity, leading to lower warpage.

c) **Thermal stability**: Glass, similar to Si, is an inorganic and high-temperature material. As such, it has a high glass transition temperature and thus is thermally stable up to about 500-700^{o}C compared to organic laminates (that are stable up to about 100-220^{o}C).

d) **Large-substrate availability**: Glass is manufactured by glass companies for display applications in thin sheets using one of the three methods: a) fusion, b) down-draw, and c) float process. The thickness of freshly drawn glass can be

engineered to a value between 30-100µm, thus eliminating the need for chemical-mechanical-polishing (CMP). CMP is an expensive process that can introduce surface defects and eventually lead to failures in glass interposers during reliability testing. The availability of thin glass panels from three different glass manufacturers: a) fusion process by Corning (Figure 9a), b) down-draw process by Schott (Figure 9b) or c) float process by Asahi Glass Company (Figure 9c) are shown in Figure 9. The thickness of all the above glass types is less than 100µm (with a minimum thickness value of 30µm).

(a) (b) (c)

Figure 9: Thin-glass substrate (30-100µm) availability, a) fusion glass by corning [20], b) down-draw glass by Schott [21], and c) float glass by Asahi Glass Company [22].

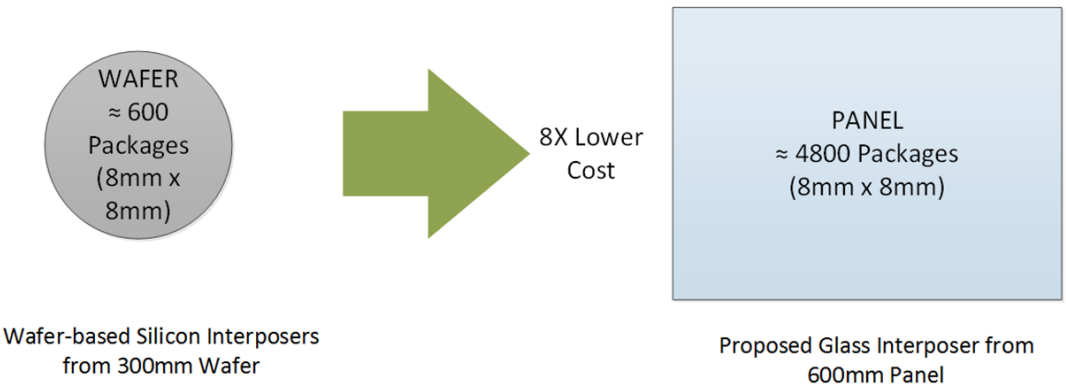


Figure 10: Productivity advantage from increased panel size, yielding more interposers per panel.

e) Low-cost of glass interposers: The low cost of glass interposers is due to two main factors; a) the use of large-area panels, yielding about eight times more interposers than with 300mm silicon wafers (Figure 10), and b) the use of low-cost materials and processes for TPVs and RDL. The material and process factors that lead to lower cost glass interposers include: a) large and thin dry films that

can be laminated with non-vacuum and high throughput package processes as opposed to expensive wafer-based BEOL processes, b) simplified double-side processes with a reduced number of process steps, c) no CMP steps, d) low temperature polymer deposition for TPV liners and build-up dielectrics and e) a minimum number of RDL routing layers on both sides of the glass interposer.

1.5 Fundamental Challenges in TPV in Glass Interposers

Although glass exhibits a number of advantages as described in the previous section, it has the following two fundamental limitations; it is a brittle material and it has very low thermal conductivity (1W/mK), about two orders of magnitude less than silicon (150W/mK). A typical stress-strain graph for glass and a material like copper is shown in Figure 11. As shown in the figure, the failure modes are different for the two materials. In the case of glass, failures occur due to brittle fracture as indicated by the red line, and the strain values are significantly smaller (0.1%) at the corresponding critical stress values. On the hand, a material such as copper undergoes ductile failure with higher strain values (10%).

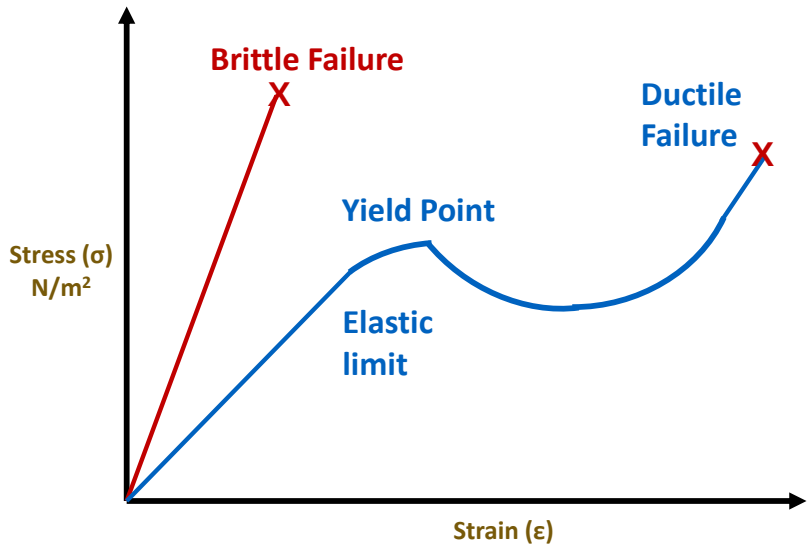


Figure 11: Typical stress-strain characteristics of glass versus metal.

These fundamental limitations give rise to many challenges in processing glass interposers that include:

a) Defect-free formation of small diameter TPV holes at small pitch
b) Reliable copper metallization of TPVs with good adhesion
c) Thermo-mechanical reliability of TPVs
d) Thermal management through the low-conductivity glass substrate
e) Assembly of ICs onto thin and brittle glass interposers and subsequent assembly onto organic package or board.

This research focuses on addressing the first two fundamental challenges, namely, a) defect-free TPV hole formation and b) copper metallization of TPVs.

Recent studies have focused on addressing some of the above challenges associated with: a) thermo-mechanical reliability of copper-plated through-vias in glass [23]; b) thermal management in glass interposers [24]; and c) glass interposers as BGA packages that are directly assembled onto printed-wiring-boards [25].

a) TPV Hole formation challenge

Glass is prone to brittle failure in the presence of ultra-small surface defects. Although freshly drawn glass has a pristine surface and thus very high strength, defects are introduced during subsequent processing steps. Griffith derived the relation between the critical stress value for failure and defect length as shown in equation 1.

$$\sigma_f = \sqrt{\frac{2E\gamma}{a\pi}} \tag{1}$$

Where, σ_f is the critical stress value at failure; E is the Young's modulus of glass; γ is the free surface energy of glass; and a is the critical defect length. According to this equation, even a 1μm size defect that can easily be created during

any of the glass interposer fabrication processes can lead to fracture at very low stresses.

Defects in glass can be introduced in many ways such as handling and via formation. A scenario wherein defects are formed in glass after laser ablation is illustrated in Figure 12. As shown in the figure an array of 100 TPVs at 100µm pitch was drilled sequentially using high power UV laser in a glass substrate having a thickness of 180µm. After laser ablation, cracks were observed both on the surface as well as in the bulk of glass. The crack formation can be attributed to the localized stress accumulation resulting from the thermal nature of the laser ablation process and low thermal conductivity of the glass substrates. In fact the formation of cracks on the glass surfaces when subjected to high power laser pulses has been studied and reported by Y. Kanemitsu and Y. Tanaka in 1987 [26]. Furthermore, the close proximity of the TPVs (small pitch) gives rise to additional challenges in defect-free TPV formation.

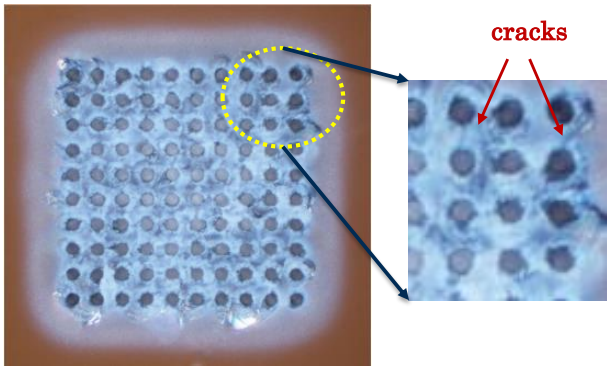


Figure 12: Top view optical image of TPV array in glass, showing crack formation after high power UV laser ablation.

b) TPV with Cu Metallization

While smooth glass surfaces without any surface defects are desirable to avoid crack initiation, they are not preferred from a metal-adhesion point of view.

Additionally, the CTE mismatch between glass (3 ppm) and copper metallization (17 ppm) results in high thermo-mechanical stresses during assembly. Such stresses can induce fatigue-related failures during reliability testing, wherein the sample is subject to alternating high and low temperatures respectively. Additionally, in the presence of surface defects, this high stress can cause crack propagation in glass, eventually leading to catastrophic failures in TPVs.

1.6 Research Objectives

The objectives of this research are twofold:

a) To explore and demonstrate ultra-small TPV-hole formation in ultra-thin glass interposers with minimal surface defects.
b) To achieve copper metallization in these holes with good adhesion and minimizing CTE-induced cracks.

Moreover, to understand the signal propagation through metallized TPVs, the electrical performance of small TPVs is analyzed through insertion loss and cross-talk simulations and measurements.

This dissertation primarily focuses on formation and metallization of ultra-small TPVs and their characterization in ultra-thin glass substrates. A schematic cross-section of the interposer proposed in this research, made of ultra-thin glass substrates with small pitch TPVs, is illustrated in Figure 13. The thickness of the proposed glass interposer is 30µm, while the desired TPV diameter and pitch are 10µm and 30µm respectively. The TPVs are metallized with copper through double-side electroless and electrolytic plating approaches.

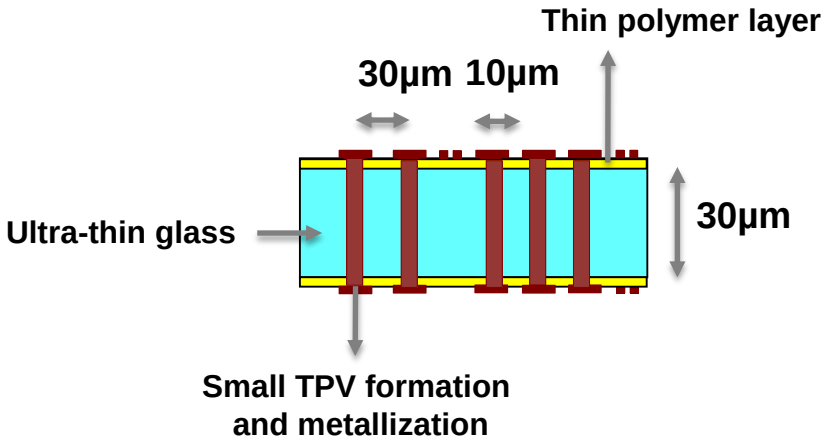


Figure 13: Schematic cross-section of ultra-thin glass interposer with fundamental focus on small pitch TPVs.

This research, for the first time, studies the formation and metallization of ultra-small TPVs in glass having 'TSV-like' dimensions. The key features and goals of this research in comparison to previous state-of-the-art research are shown in Table 2.

Table 2: Proposed research versus state of art

Parameters	State of the Art	Proposed Research
Glass Thickness	100 – 500 µm	30µm
TPV Diameter	50 – 200 µm	10µm
TPV Pitch	100 – 500 µm	< 30µm
Process Methods	Wafer-based Bare Glass	Panel-based Polymer on Glass

1.7 Proposed research to achieve objectives

This dissertation is organized into seven chapters. Each chapter begins with a theoretical basis of fundamental principles followed by processes, characterization and analysis.

In this chapter, the need for 3D interposers requiring ultra-small TPVs using glass as the interposer material was discussed. The next six chapters are organized as follows:

CHAPTER 2: In chapter 2, the relevant prior research on TPV formation, metallization, and characterization in glass substrates is presented.

CHAPTER 3: In chapter 3, the electrical design of ultra-small TPVs in thin glass is discussed. Based on the simulation results, design guidelines are outlined for subsequent via formation and metallization tasks.

CHAPTER 4: This chapter is divided into two sections. In the first section, several TPV formation methods are investigated from a fundamental perspective. These include mechanical processes, photo-chemical etching, and laser ablation. Based on these studies, process guidelines for defect-free TPV formation are established.

In the second section, excimer laser ablation (193nm) is studied for achieving ultra-small TPV holes in 30µm thin glass substrates.

CHAPTER 5: In chapter 5, the metallization of TPVs in glass using double-side electroless and electrolytic copper deposition is studied. Additionally, the thermo-mechanical behavior of Cu-plated TPVs is analyzed through thermal cycle tests (TCT). The results from failure analysis are also discussed.

CHAPTER 6: In this chapter, the electrical behavior of small TPVs is analyzed through insertion loss measurements. Additionally, fabrication of multi-layer glass interposers and implementation of RF filter devices are presented.

CHAPTER 7: The last chapter summarizes the key findings, research contributions, and potential extensions of the research presented in this dissertation.

Chapter 2

PRIOR ART

The previous chapter established a compelling need for high density interposers with fine pitch TPV and defined the research objectives as well as the fundamental challenges associated with TPV in glass interposers. The two major challenges identified were: a) defect-free TPV hole formation and b) reliable TPV metallization in ultra-thin glass substrates. This chapter will provide a comprehensive review of published literature addressing these two challenges. The final section in this chapter will present a summary of published work on glass interposers with particular emphasis on the electrical modeling and characterization of glass TPVs.

2.1 Prior work in TPV formation

This section describes prior work on the formation of through vias in glass substrates by a wide variety of techniques over the past several years. The fundamental barrier to thin glass interposers is the defect-free formation of small vias in close proximity to each other (small pitch). The brittleness and chemical inertness of glass make it difficult to machine through-holes at small pitch. Early methods for glass micromachining, such as sandblasting, are limited in their ability to achieve small via dimensions, and a number of recent methods have been pursued to reduce the via diameter and pitch of TPVs in glass. However, there is limited published work in the formation of TPVs at ultra-fine pitch below 100µm in ultra-thin glass below 100µm, which is the main focus of this research study.

a) Sandblasting:

Sandblasting was one of the earliest methods used to machine glass, and this technique has been significantly improved in recent work on RF MEMS by Y.K. Park [27]. Park formed TGVs with a diameter of 200µm in 500µm thick glass substrates

with a via taper angle of 15 degrees. Due to the limitations in focusing the sandblasting nozzle output to smaller spot sizes and also due to the lateral damage induced during machining, it would be difficult to reduce the via diameter and pitch further. Also, the smallest feature size is limited by the minimum size of the abrasive particles (typically about 20-50µm).

b) Glass reflow over metal posts:

J.Y. Lee et. al. investigated a glass reflow process to achieve conductive through vias in glass for wafer level RF MEMS application [28, 29]. In such a reflow process, low resistivity silicon was patterned using DRIE and used as the underlying substrate for glass reflow at a temperature of 1025^{o}C. The patterned silicon posts were subsequently etched away to form through vias in glass. A bottom-up plating approach was used to metallize the vias using copper electroplating. Finally, CMP was performed to reveal the TGVs. The diameter and pitch of TGVs reported using the glass reflow process were 40µm and 140µm respectively.

NEC Schott has demonstrated and commercialized a similar technique using a wafer-based glass interposer with vertical tungsten feed-throughs [30]. It was shown that by flowing molten glass over tungsten plugs, vertical interconnections could be achieved with good surface planarity. Such an approach integrates via formation and metallization into a single step. The use of tungsten as the metallization material resulted in significantly lower thermo-mechanical stresses during the high temperature glass-flow process due to a close CTE match between tungsten and the glass substrate. Tungsten vias with a minimum diameter of 100µm were formed using this approach.

Although the above reflow process helped achieve glass substrates with metallized TPVs, there are two challenges with this approach, a) the high

temperatures required for glass reflow result in higher stress and b) the need for CMP to reveal the back side of TPVs can result in glass cracking. Additionally, the high viscosity of the glass melt limits the minimum TPV pitch to values greater than 100µm.

c) Photosensitive Glass:

The ability to introduce photosensitive compounds into the glass formulation has attracted a great deal of attention due to the potential for the formation of millions of TPVs in a glass wafer or panel all at the same time as opposed to the other serial process methods described in this chapter. Hoya Glass demonstrated a process to fabricate wafer-based glass interposers using photo-definable glass [31]. In this process, via regions in the glass are selectively illuminated by UV light, and in the subsequent high temperature sintering step, the UV irradiated regions are converted to ceramic phase. Finally, the glass substrate is etched in a HF solution. The ceramic regions gets etched away with higher selectivity and 10-20 times faster than the unexposed glass regions, resulting in high aspect ratio TPVs. Through vias having small diameters down to 25µm were achieved in photo-sensitive glass substrates with a glass thickness of 100µm. Via metallization was achieved using sputtered-copper seed-layer followed by electroplating. However, the size of the glass wafer was limited to 120mm.

d) Electric discharge:

Researchers at Asahi Glass Company (AGC) have developed an electric discharge method to form through vias in glass [32]. Dielectric breakdown in glass occurs when a very high electric voltage is applied between across the two ends of the dielectric. This causes melting and vaporization of the glass material and results in through via hole formation. Minimum via diameters of 30-60µm in 100µm thick glass

substrates were reported. Even though the electric discharge method is a serial process, faster processing time of 300μs for a single via has been achieved, leading to an overall throughput value of greater than 1000 vias per second. The resulting side-wall profile was observed to be slightly tapered with slight rounding around the via entrance.

e) Deep Reactive Ion Etching (DRIE):

DRIE based on SF_6 plasma was used to form vertical feed-through in glass at larger pitch (> 300μm) for MEMS applications [33-36]. The etch rates in glass are slower (~ 0.6μm/min) compared to TSV etching in CMOS grade silicon. Higher etch rates can be achieved by a) reducing the gas pressure, b) increasing the self-bias voltage and glass flow within the reactive-ion chamber. Although DRIE is the primary method used to produce TSVs in silicon, the adoption of DRIE to glass requires further innovations in large panel etching tools and higher throughput processes.

f) Laser ablation:

Laser ablation techniques have emerged as the primary choice for forming fine pitch TPVs in glass, and a number of laser methods have been studied. Adela Ben-Yarkar and Robert L. Byer have examined femto-second laser ablation properties of borosilicate glass by studying the single-shot and multi-shot ablation threshold values [37, 38]. The ablation phenomenon was observed to be almost wavelength independent. High peak intensities associated with ultra-short laser pulses initiate non-linear absorption of incident photons, leading to glass material removal.

Ying-Tung Chen et al. studied nanosecond excimer laser ablation in glass using a mask projection method [39]. The glass surface morphology was studied as a function of repetition rate, and the results in glass were compared to those obtained in

polyimide and silicon. Prior work on excimer laser ablation in glass has been limited to via formation in thicker glass substrates (500µm) [40-42].

In addition to excimer and femto-second lasers, a number of research studies have investigated CO_2 laser ablation for via formation in 500µm thick glass substrates [43-46]. Brusberg et al. studied CO_2 laser ablation in 500µm thick D263Teco glass substrates. The study showed that TPVs with a diameter of 100µm were formed in 0.25 seconds; however, cracks were reported after thermal cycling in almost half the TPVs [43]. Thermally induced stress was cited as a potential reason for failure. To reduce the thermal stress generated during CO_2 laser machining, a water assisted ablation approach was studied by Chung C.K et al. [44]. In addition to water assisted etching, the researchers investigated thick poly-dimethylsiloxane (PDMS) layers on glass prior to glass machining [46]. The PDMS layer was reported to reduce the temperature gradient and heat-affected-zone after CO_2 laser ablation. A recent study from Mitsubishi Electric reported the formation of small diameter TPVs (25µm) using CO_2 laser ablation in 0.1mm thick glass substrates [47]. The formation of small TPVs in glass was attributed to two reasons: a) ultra-short pulse width of lasers that reduced the amount of heat generated in the ablation region, and b) surface treatment methods that reduced the enlargement of the TPV holes, especially on the entrance side.

g) Laser Assisted Etching:

Nukaga, O et al. studied the fabrication of three dimensional TPVs in glass using a laser assisted wet etch process [48]. A femto-second laser operating at 800nm was first used to selectively modify the glass surface through multi-photon absorption. Next, the laser modified regions were preferentially etched using diluted HF solution. The study showed that through channels can be achieved with a minimum feature size of 15µm using the above method.

Corning has developed a method to form vias in glass at high through-put [49]. The minimum diameter of vias achieved was 30µm in 150µm thick glass substrates. To improve the strength of glass wafers with vias, Corning has patented a method of introducing compressive stresses on the glass surface [50]. The introduction of compressive stresses was achieved through an ion-exchange process. The fracture toughness of glass with vias was reported to have significantly improved after the exchange process.

A summary of the methods to form TPVs in glass is shown in Table 3 along with the smallest dimensions achieved by each method.

Table 3: Summary of TPV formation methods

References	**TPV method**	**Dimensions (diameter/pitch)**
Y.K Park et.al	Sand-blasting	200 (µm)
JY Lee et.al NEC Schott	Glass reflow process - Copper - Tungsten	 40/140 (µm) 100 (µm)
Hoya Glass 3D Glass solutions	Photo sensitive glass	25 (µm)
Asahi Glass Company	Electric discharge	30 (µm)
T. Akashi et.al L. Li et. al X. Li et. al	DRIE (SF_6 /C_4F_8)	100 (µm)
	Laser ablation	
A.B Yarkar	- fs laser	40 (µm)
Y.T Chen et.al, D. Bhatt et.al, K. Berndet.al, A.A. Tseng et.al	- Excimer laser	100 (µm)
L. Brusberg et.al, C.K Chung et. al, S. Yu et. al	- CO_2 laser	100 (µm)
O. Nukaga et. al	Laser assisted etching	15µm features
Corning Glass	Corning propriety method	30 (µm)

While it is clear that thinner glass would result in the formation of smaller TPVs with shorter processing times and overall reduce the thermal and mechanical damage to glass; migrating to thinner glass poses handling challenges in manufacturing because glass is prone to brittle fracture in the presence of surface defects. To further validate the fact that thinner glass can lead to smaller TPV holes, a recent study by Coherent Laser has shown the formation of ultra-small through holes in thin glass substrates using 193nm excimer laser ablation [51]. Although handling can be classified as a manufacturing challenge, the following section provides a brief summary of thin glass handling methods that have been developed primarily for display applications.

2.2 Thin glass handling methods

Most of the prior work on glass interposers has focused on thicker glass substrates (300-500µm) with process steps implemented on bare glass. In contrast, this research studies and explores ultra-thin glass (< 100µm) for interposers using novel polymer dielectrics on the glass surface for improved handling. The use of polymeric coatings on glass for handling is well known in the display industry. This section outlines some of the thin-glass handling methods reported in the literature.

a) Bare glass handling

Ultra-thin glass substrates are readily available in large panel format and actively used for display applications [52, 53]. Asahi Glass Company in Japan has developed a thin-glass (0.1mm) handling method using thicker glass as carrier substrates [54]. The thickness of the carrier substrate is typically 500µm or higher. Such an approach enables application of standard display processes to thin-glass, thereby reducing the probability of defect growth and failures during manufacturing. Additionally, Corning has performed a comparative study on the fracture toughness of

glass and silicon wafers [49, 55]. Prior studies have shown that failures in glass and silicon substrates are a function of defect density within the material [56], and the strength of glass wafers was characterized using ring on ring tests. The resulting weilbull distribution plot showed repeatable performance in the case of glass with strength values varying between 300-500MPa. In summary, the strength of glass wafers is highly dependent on the defect density and can at times be comparable or has improved strength characteristics than silicon wafers.

b) Polymeric coatings on glass

The use of thin organic polymer films have been reported to increase the strength of thin glass substrates [57-60]. Improvement in handling using polymer can be attributed to the following three reasons: a) protection of the glass surface from physical and chemical damage; b) polymer conforming over surface defects, resulting in so called 'defect healing' in which the polymer arrests crack growth; and c) introduction of compressive stress onto the glass surface. The effect of polymer coatings on glass surfaces subjected to indentation loads has been studied [61, 62]. The lower modulus of the polymer was reported to cause reduction in the indentation stresses generated on the surface of the glass.

2.3 Prior work in TPV metallization

Direct metallization on glass is a significant challenge due to its chemical inertness and smooth interface. In addition, the thermo-mechanical stresses that arise due to the CTE mismatch between glass and metallization material can cause reliability failures in the metallized TPV. Copper is commonly used as the metallization material owing to its high electrical conductivity. TPV metallization can be achieved using the following methods:

- Electroless deposition

- Sputtering (Physical Vapor Deposition - PVD / Chemical Vapor Deposition - CVD)
- Alternate conductor fill (tungsten or copper)

a) Electroless Deposition:

Electroless deposition of copper is an effective and low-cost approach that can be scaled to large substrate processing. David Hutt et al. [63] examined the electroless deposition of copper directly on glass using silane-based self-assembled monolayers (SAM). The amine functional groups (NH_2) within the silane molecule (3-aminopropyltrimethoxysilane) provide adhesion between the palladium and tin catalysts and the glass surface. The catalysts facilitated redox reactions within the plating solution, resulting in a thin metal layer on the glass surface. In another work, electroless copper deposition was achieved by functionalizing the glass surface using silane and graft polymerization of aniline [64]. The resulting surface chemistry provided good adhesion between glass and the palladium catalyst, which facilitated electroless copper deposition.

Xiaoyun Cui et al. [65] characterized an electroless copper deposition process on silane treated glass as a function of the plating time, temperature, and copper surface profile. The study utilized surface characterization methods and revealed adhesion failures at the interface between the copper and catalyst. To improve the bonding strength, the researchers also investigated the impact of excimer laser-induced surface roughness on the adhesion of copper seed layer [66]. Laser-induced surface roughness coupled with silane treatment helped improve the adhesion strength between copper and glass. In addition to silane treated glass, the nature of glass surface topology on plated copper adhesion was studied by Baofeng He et al. [67]. Glass surface roughness was induced using a KrF (248nm) excimer laser system.

Bead blasting was also employed to create a rough topology on the glass surface. Scratch tests were performed to study the adhesion of copper as a function of the glass surface roughness. Adhesion strength was reported to have improved as the surface roughness increased.

Selective metallization on laser modified photo-sensitive glass surface was reported by Koji Sugioka and co-authors [68]. Femtosecond lasers were used to initiate non-linear absorption on the glass surface that resulted in the generation of free electrons. These free electrons caused reduction of the metal ions near the glass surface, resulting in precipitation of metal onto the laser irradiated glass surface. Jian Xu et. al. [69] studied in detail the mechanism involved in laser assisted metallization on glass. In the laser assisted metallization approach, glass coated with silver nitride was exposed to femto-second laser irradiation, which caused the silver atoms to be deposited on the glass surface. These silver atoms acted as a seed layer for subsequent metallization.

Direct metallization on glass has been studied for thin-film-transistor (TFT) fabrication [70, 71]. NiB or copper was deposited using an electroless process and patterned using a lithography step. The thickness of the plated metallization was in the order of a few hundred nano-meters.

Direct plating of copper on glass for interposers was recently reported by Simon Bamberg et al. [72]. According to Bamberg's report, an electroless copper seed layer was deposited on the bare glass surface using various surface roughening techniques, including surface conditioning and chemical pretreatment.

b) Sputtering and Vacuum Deposition

The deposition of thin metal films directly on glass using chemical-vapor-deposition (CVD) or physical-vapor-deposition (PVD) techniques is very well understood.

Chen et al. studied thin-adhesion layers on glass by sputtering titanium-tungsten (TiW), titanium (Ti), chrome (Cr) or copper (Cu) layers with a thickness of 120nm [73]. It was reported that TiW showed the highest adhesion strength of these metals, and the optimum thickness of the TiW layer was determined to be 50nm.

To achieve complete seed-layer coverage without discontinuity inside high aspect ratio (10:1) TPVs in glass, Ogutu et al. investigated a hybrid method using sputtering and electroless deposition [74]. Initially, a thin Ti-Cu layer was sputtered followed by electroless plating of nickel. Such a hybrid approach combines the benefits of sputtering for their high adhesion strength with the electroless deposition process to bridge the voids in the seed layer caused by the limitations of sputtering in high aspect ratio vias.

Wang and co-authors from Corning studied via metallization in glass using sputtering [49]. A thin layer of tantalum was sputtered using PVD prior to copper seed layer deposition. Copper electroplating was used to subsequently metallize the glass vias to the desired thickness.

c) Alternate TPV Fill

Asahi Glass Company and Triton reported on a process to metallize through vias in glass with copper paste filling for 2.5D and 3D glass interposers [75, 76]. The through vias in glass were formed using the electric discharge method, which yielded TPVs with a minimum via pitch of 60µm in 100µm thick glass substrates. The through vias were subsequently metallized using conductive metal paste, e.g., Cu-

paste. The study showed that the CTE of the Cu-paste could be adjusted to a value similar to that of the glass substrate to achieve higher reliability. Although Cu-paste filling has been proposed as a lower cost-alternative to copper plating, the conductivity of the Cu-paste is much lower (1.6 to 1.9 m Ohm/sq.) compared to plated copper, that may affect the electrical performance of TPVs.

2.4 Prior Work in Glass Interposers

Glass as an interposer technology has attracted attention in the recent past due to its favorable material properties. Although most of the interposer research has focused on TSVs in silicon, a few groups have studied glass interposers. This section provides an overview of the integration processes used to form TPVs and RDLs for glass interposers pursued in industry and academia.

The lamination of multiple layers of thin glass to achieve glass interposers was studied by researchers at the University of Loughborough in UK [77, 78]. Glass sheets with 100µm thickness were used for the lamination study. The study showed that reliable bonding between the glass sheets was achieved at relatively low temperatures (200-300^{o}C) and pressure values (1-3MPa) [79]. In the above study, through vias in glass were formed using 248nm KrF-based excimer lasers, and a minimum via diameter of 40µm was reported in 50µm thick glass substrates. In addition, the study revealed that an increase in laser fluence from 3 J/cm^2 to 4.5 J/cm^2 resulted in a reduction of via taper angle from 19 degrees to 14 degrees [40]. Metallization of vias and conductive traces on the glass surface was achieved using electroless copper seed-layer deposition. To achieve improved adhesion between the electroless deposited copper and glass, a chemical consisting of silane molecules (3-aminopropyl trimethoxy silane) was used to functionalize the glass surface [66]. It was observed that the silane treatment helped increase the bond strength between

glass and the catalyst (palladium or tin); however, adhesion failures were observed during tape peel testing when seed-layer thickness exceeded 150nm.

Fraunhofer IZM explored glass-based electronic and photonic modules [80-82] with through-glass-vias (TGVs) fabricated using femto-second and excimer laser ablation. The glass substrates used for the TGV study had a thickness value of 400µm or 500µm to facilitate handling during processing. The TiSa femtosecond (fs) laser helped achieve through holes with an entrance diameter of 99µm in 500µm thick glass. On the other hand, TGV formation using excimer lasers with nano-second pulse duration yielded smaller via diameter at the entrance (48µm) compared to fs lasers [81]. This implies that the highest aspect ratio of TGVs achieved using the above ablation techniques was approximately 5:1. Sputtered and electroless copper deposition were used to form the conductive seed layer for direct metallization on the glass surfaces. In addition to the electrical interconnections, optical waveguides were fabricated on the glass surface through an ion-exchange process using silver ions. The silver ions replaced the sodium within the glass matrix and provided a graded refractive index necessary for optical wave confinement. The work on such photonic modules has focused on thicker glass substrates (400-500µm), which are significantly easier to process compared to the ultra-thin glass substrates (30-100µm) proposed in this research.

ITRI in collaboration with Corning have investigated the fabrication of glass interposers using wafer-based processing methods that are commonly used for silicon interposer fabrication [83, 84]. Through vias with a diameter of 30µm were formed in 100µm thin glass substrates by Corning. Subsequent metallization of the TPVs was achieved using a combination of sputtered seeding (Ti+Cu) and copper electroplating. Wafer thinning was performed on the glass substrates to reveal the TPVs on the back

side and RDLs were lithographically patterned after flipping the glass wafer. PBO was used as the passivation layer between RDL layers on each side of the interposer. The line width on the RDL layers was limited to a minimum value of 20µm in the above study.

A recent study on thin glass interposers by TSMC demonstrated the ability to process a 50µm thin glass substrate using a thicker silicon wafer as the carrier substrate [85, 86]. The diameter of the carrier wafer was 300mm. Vias were formed in glass using laser ablation, and a minimum via diameter and pitch of 25µm and 45µm respectively were reported. The vias were subsequently metallized with copper, and the overburden was removed using chemical-mechanical-polishing (CMP). However, the key challenges identified in the report included: a) void free bonding between glass and silicon and b) glass cracking during CMP. Moreover, the use of carrier substrates limits the processing to single side and increases the process steps and complexity.

Table 4 summarizes the results of prior work on glass interposers. As shown in Table, the focus of previous research in glass has been on thicker glass or on wafer processing with carrier wafers and single sided processing. The unique contribution of the research in this dissertation is that it explores novel methods for double-side processing of ultra-thin glass interposers with fine-pitch metallized TPVs.

Table 4: Summary of prior work on glass interposers

Research Group	References	Results summary
Loughborough University	[40, 66, 77-79]	Multi-layer laminated glass, with 100µm dia. TPV
Fraunhofer IZM	[80-82]	Laser ablation in 400-500µm glass substrates, with TPV aspect ratio of 5:1
ITRI and Corning	[83, 84]	Wafer Process, 30µm dia. TPV in 100µm glass Sputtered seed layer and electroplating
TSMC	[85, 86]	25µm dia. TPV in 50µm glass using Si carrier

2.5 Previous work on electrical modeling and characterization of TPVs in glass

The high electrical resistivity of glass enables efficient transmission of signals with minimal insertion loss and cross-talk. Although the signal propagation through TSVs has been studied in detail through analytical models and simulations, the behavior of through-vias in glass has been studied to a lesser extent. This section outlines some of the prior work on electrical modeling and characterization of through vias in glass.

3D full wave EM solvers have been used to study the insertion loss and cross-talk behavior of TGVs at higher frequencies [30, 87, 88]. The thickness of the glass substrates were greater than 100µm, and tungsten was modelled as the via fill material. The electrical behavior of TPVs (via parasitic, insertion loss, NEXT and FEXT) in polymer laminated glass substrates has been studied by T. Bandyopadhyay in his PhD thesis through modeling and characterization, taking into account TPV geometry and polymer material variations [89]. The thickness of the glass substrate used for modeling and characterization was 75µm-180µm with TPV diameter greater than 30µm.

TGVs in glass have been modelled to study the high frequency characteristics for RF applications. The low loss associated with glass vias was exploited to design RF filters and phase-shifters using MEMS [28, 29, 90, 91].

A recent study on the electrical modeling and characterization of through-glass-vias (TGVs) is reported by C. Kim and Y.K. Yoon from the university of Florida [92]. In their work an equivalent circuit model (π-model) was proposed and the TGVs were characterized by studying the parametric variations in geometry and corresponding variations in RLGC values of TGVs.

Since glass has higher impedance compared to silicon, via transitions in multi-layer (4 or greater) cause resonances between power-ground planes [89, 93]. This is one of the key challenges in glass interposers that need to be addressed to achieve optimum signal and power integrity.

Most of the prior work on electrical modeling has focused on thicker glass substrates with larger via diameters (> 30µm). The proposed research extends some of the work reported in literature by studying the signal integrity of small-pitch vias (< 30µm) in two-metal layer, ultra-thin glass substrates (30-50µm). Signal insertion loss and cross-talk between small pitch TPVs are modelled in HFSS, and the results obtained are corroborated with measurements.

Chapter 3

ELECTRICAL MODELING AND DESIGN OF TPVS IN GLASS

In this chapter, the electrical characteristics of small TPVs in glass at fine pitch are studied using 3D simulations. The electrical parameters that were analyzed using full wave electromagnetic (EM) modeling in the frequency domain are: a) signal insertion loss and b) TPV to TPV coupling (i.e., cross-talk).

3.1 3D EM simulation – Comparison between TPVs in Glass and TSV

A 3D model was developed using a full-wave EM solver (HFSS) to compare the insertion loss and cross-talk behavior of TPVs in glass and TSVs in silicon. The geometry of the TPV and TSV structures used in the modeling study is shown in Figure 14. For the glass TPVs, vertical vias with a diameter of 15µm were modeled in ultra-thin (30µm) borosilicate glass (ε_r = 6.7; tan δ = 0.006) with 3µm thin polymer (Zeon Insulation Film - ZEONIF^{TM}) (ε_r = 3.1; tan δ = 0.005) on both sides. The interconnections were modeled as fully-filled copper vias with capture pads on both sides.

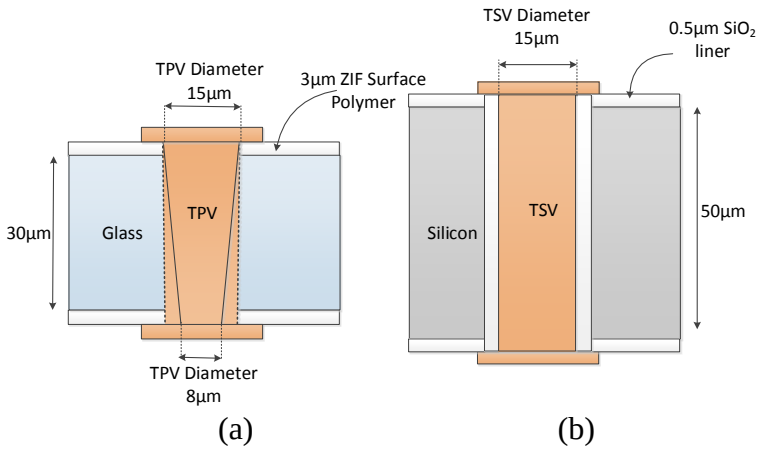


Figure 14: Schematic cross-sections showing interconnect geometries used for electrical modeling of: a) TPV in glass and b) TSV in silicon.

The TSVs in 50µm thin silicon substrate (ε_r = 11.9; conductivity = 10 S/m) were modeled as vertical interconnections with an oxide liner thickness of 0.5µm. To obtain the insertion loss of TPVs and TSVs, a lumped port excitation was defined at the edge of the signal pads on the top and bottom side of the vias in a ground-signal-ground (GSG) configuration. The insertion loss plots obtained from the simulations shown in Figure 15 indicated a low insertion loss (< 0.05dB till 40GHz) for glass (blue line), which can be attributed to the high electrical resistivity (> 10^{10}Ωm) of glass. On the other hand, the modeling results for silicon (red line) showed a significantly higher loss (> 0.3dB at 20GHz) due to the semiconducting nature of the substrate (0.1-10 Ωm) and the lower impedance of oxide capacitance (SiO_2 liner) in the TSVs.

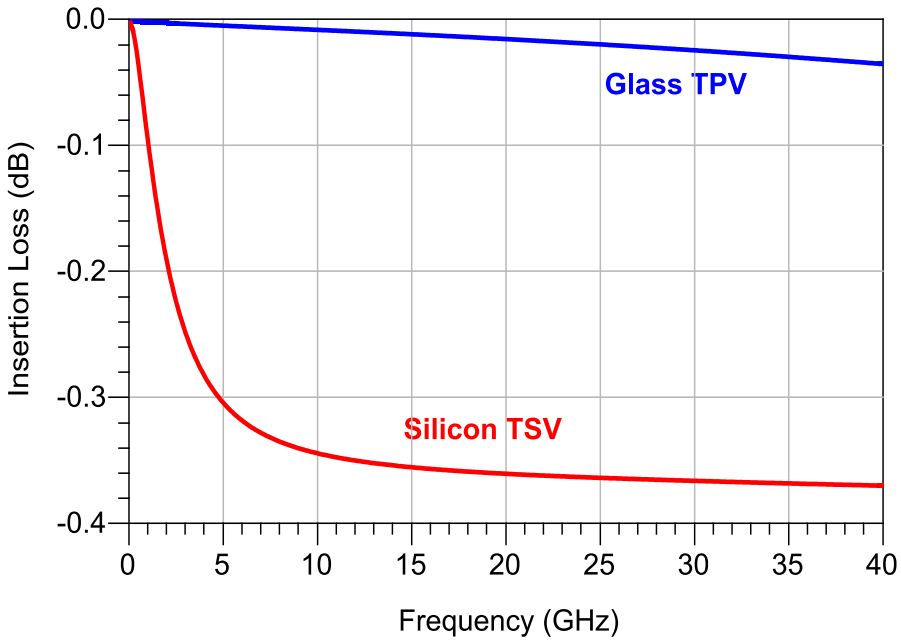


Figure 15: Simulated insertion loss (S_{21}) of TPV and TSV interconnections.

To study the cross-talk between closely spaced vias, TPVs in glass and TSVs in silicon having a GSSG configuration were modeled in HFSS, using the same geometry that was used to study the insertion loss. The GSSG configuration of these

models included a via-to-via spacing of 15µm. Moreover, the TPVs in glass were modeled as conical structures in this study. The simulated near-end-cross-talk (NEXT) and far-end-cross-talk (FEXT) responses are shown in Figure 16. As the blue lines indicate, it was observed that the TPVs in glass exhibit higher isolation (greater than 37dB until 20 GHz) compared to the TSVs (30dB at 20GHz) for the same via to via spacing (15µm). The higher degree of signal isolation and reduced coupling between the adjacent TPVs can be attributed to the ultra-high resistivity of the glass substrate and its lower dielectric constant (ε_r =6.7) compared to silicon (ε_r =11.9).

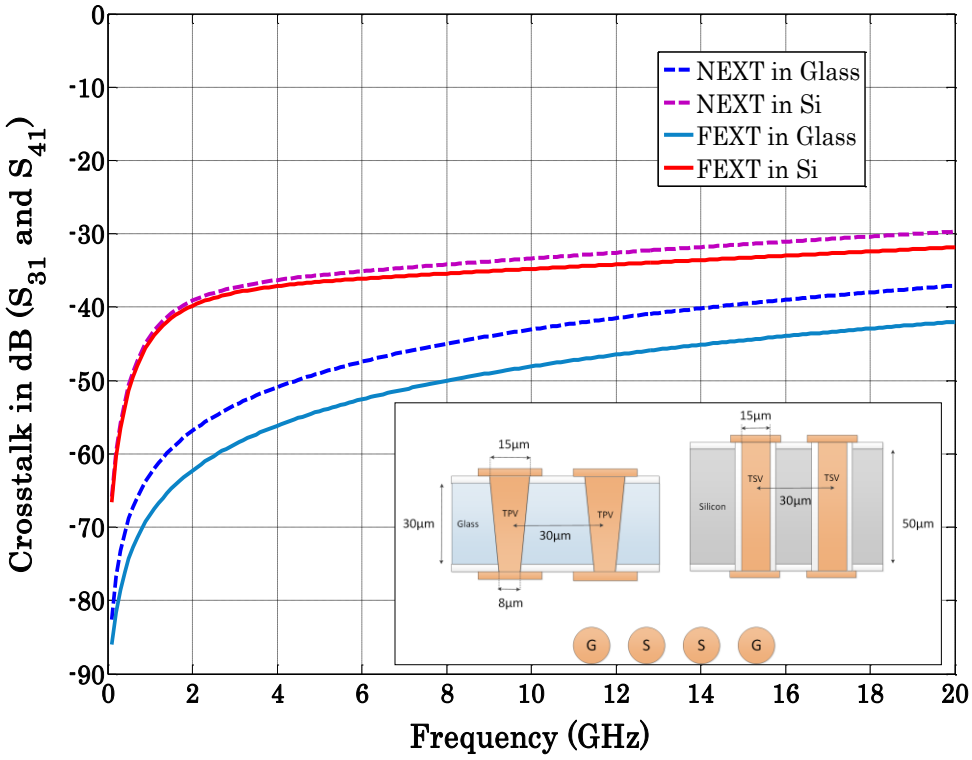


Figure 16: Simulated NEXT and FEXT response in TPVs and TSVs.

Thus, the results from the electrical modeling of TPVs and TSVs suggest that TPVs in glass can be used for signal transmission at high frequencies with lower insertion loss and cross-talk characteristics compared to TSVs in silicon interposers.

3.2 TPV insertion loss – parametric study

In an effort to understand the effect of material and process variations on the insertion loss of glass TPVs, a parametric study was conducted. The following material and process-induced variations were included in the study:

a) Effect of TPV taper
b) Effect of change in glass material properties
c) Effect of change in TPV conductor material
d) Metallization thickness and plating profile variations

a) Effect of TPV taper

In case of the glass TPVs, a tapered via was modelled with 15µm entrance and 8µm exit diameters to study the effect of via-taper on signal propagation. Analyzing the effect of taper on via performance is important because certain processes that are used to form TPV holes in glass (e.g., laser ablation) result in a tapered side-wall profile. This taper angle is a function of material and process parameters, including the glass composition, glass thickness, laser fluence and number of laser pulses. Therefore, to better understand the effects of taper on the electrical characteristics, the TPV models were updated to conical structures.

The simulated insertion loss of vertical and tapered TPV is shown in Figure 17. It was observed that the loss associated with tapered TPVs (blue line) was slightly higher compared to vertical vias, which can be attributed to the higher inductance of the tapered TPV caused by an increase in concentration of current in the periphery of the conductor (skin effect). Both the vertical and tapered TPVs showed very low insertion loss (< 0.03dB) up to 40GHz.

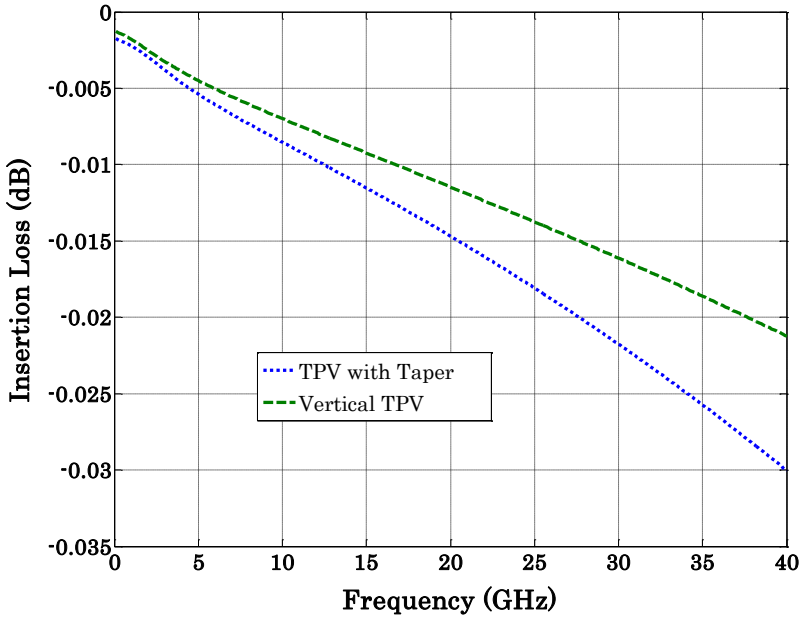


Figure 17: Simulated insertion loss (S_{21}) of vertical and tapered TPV in glass.

Updated TPV model with Via Taper for studying: b) Effect of change in glass material properties, c) Effect of change in TPV conductor material and d) Metallization thickness and plating profile variations

To capture the effect of material and process variations on the electrical behavior of tapered TPVs, new TPV models were created having conical structures with entrance and exit diameters of 10µm and 6µm respectively, and the pad size was defined to be 20µm. These dimensions were determined based on initial process experiments discussed later on in Chapter 4. The geometry used in the modeling study is illustrated in Figure 18. The signal TPV along with two surrounding ground TPVs were modelled with a via-to-via spacing of 20µm. A lumped port excitation was defined at the edge of the signal pads on the top and bottom sides of the signal via and a discrete frequency sweep was used to compute the S-parameters. The simulations were performed until 40GHz with a step size of 100MHz. TPV models with the same basic geometry and configuration (GSG) were used to study the insertion loss with

changes in glass material properties, conductor material properties, and copper metallization thickness.

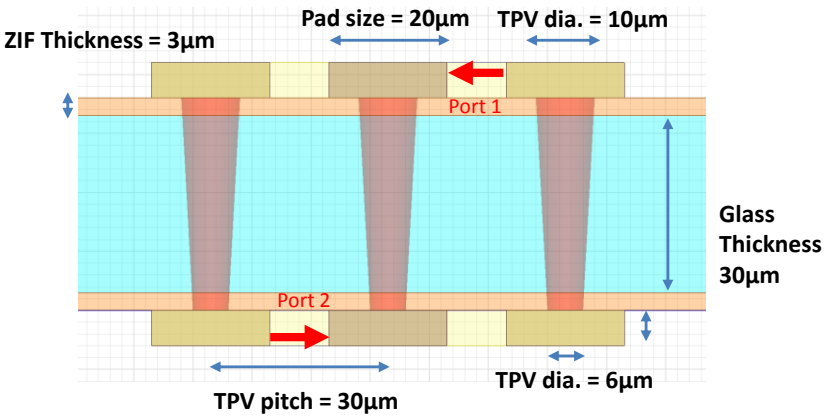


Figure 18: Cross-section view of TPV model in 30µm thin glass used in the modeling study.

b) Effect of change in glass type on TPV insertion loss

In the case of glass interposers, it may be necessary to engineer the CTE value of glass to achieve optimum thermo-mechanical reliability of interconnections from the die to interposer and interposer to printed wiring board. This variation in CTE can be achieved by changing the glass composition. However, such variations in glass composition can cause slight modifications in the electrical properties of the glass material. Therefore, it is important to understand the effect of such changes on the signal propagation through TPVs.

To determine the effect of a change in glass properties on insertion loss in TPVs, two different glass types were included in the model, AF32 and D263 from Schott AG, Germany, with a 3µm thin polymer layer (Zeonif ZS-100 from Zeon Corporation, Japan, herein referred to as ZIF) on both sides. Both the AF32 and the D263 are available at a minimum glass thickness value of 30µm. The electrical properties of the two different glass types are summarized in Table 5.

Table 5: Electrical properties of Glass and polymer materials used in the modeling study

Material	Dielectric constant	Loss tangent
Glass (D263)	6.7	0.0061
Glass (AF32)	5.1	0.0028
ZIF (polymer)	3.1	0.005

The insertion loss plot of a fully metallized (with copper) via in AF32 and D263 glass types with a thickness of 30μm is shown in Figure 19. The higher loss tangent value of D263 glass (ε_r = 0.0061) resulted in a relatively higher insertion loss value compared to AF32 (ε_r = 0.0028). However, the insertion loss in both cases was less than 0.06dB till 40 GHz, which is significantly lower compared to TSVs in silicon (> 0.3dB at 20GHz). Additionally, the simulated return loss was observed to be lower than 19dB until 40 GHz, as shown in Figure 20. In Figure 20, it can be observed that the return loss plot indicates higher reflections for TPVs in AF32 glass. This can be attributed to the lower loss of AF32 leading to smaller attenuation of the reflected signal.

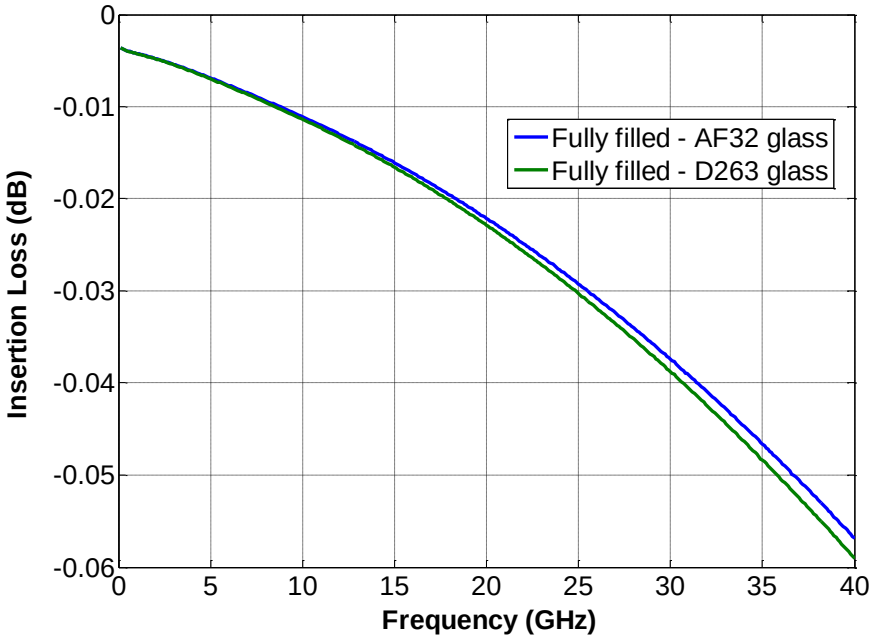


Figure 19: Insertion loss of TPV as a function of change in glass material.

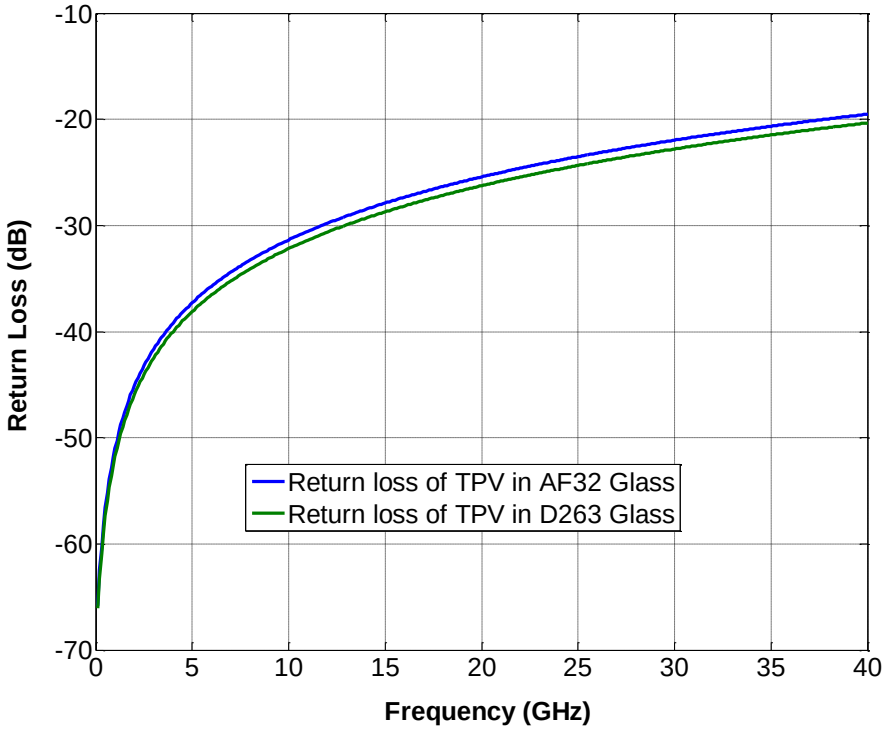


Figure 20: Return loss of TPV as a function of glass material.

c) Effect of change in TPV conductor material

It may be desirable to vary the conductor material inside TPVs for the following reasons: a) to achieve good thermo-mechanical reliability of TPVs by reducing the stress induced by a CTE mismatch between the glass and the conductor material or b) to develop a high throughput process for TPV metallization. The change in conductor material impacts the electrical characteristics of TPVs due to the change in resistivity of the conductor material.

To study the impact of changes in TPV conductor material on signal propagation, TPVs filled with different materials were modeled using the same geometry as explained in the previous section. Copper, tungsten, aluminum, and solder were studied as the conductor material. The vias were modeled as fully metallized TPVs with a pad thickness of 8μm. The simulated insertion loss plot is shown in Figure 21. Copper has the highest conductivity of the materials chosen and thus shows lowest insertion loss. However, it can be observed that the loss associated with the other materials is still significantly lower compared to TSV with copper metallization with an oxide thickness of 0.5μm, as shown in Figure 22. The lower insertion loss of TPVs in 30μm thin glass can be attributed to: a) the ultra-short interconnect length, b) the high resistivity of the substrate, and c) the absence of oxide capacitance (which is present in case of TSVs) around the TPV sidewall.

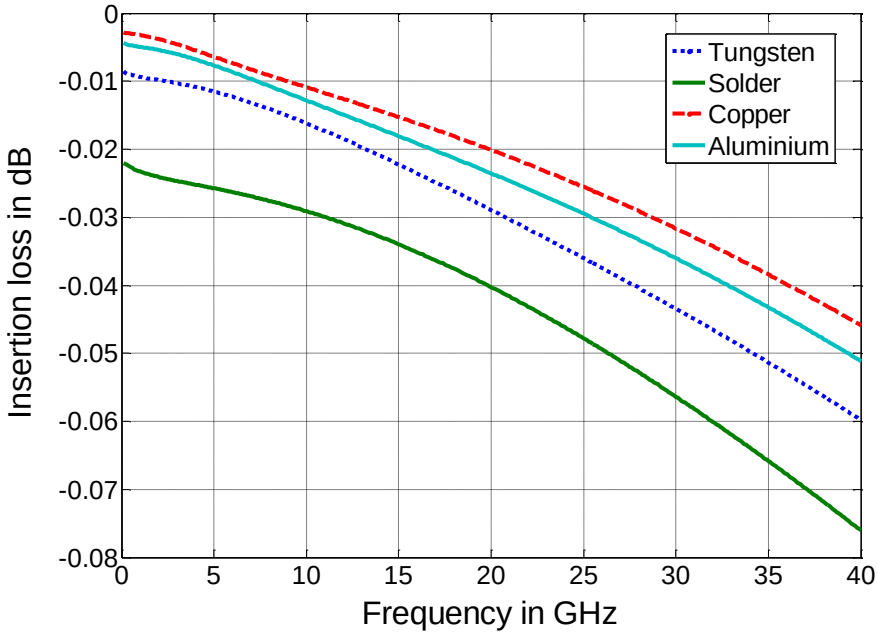


Figure 21: Insertion loss of TPV as a function of different conductor materials.

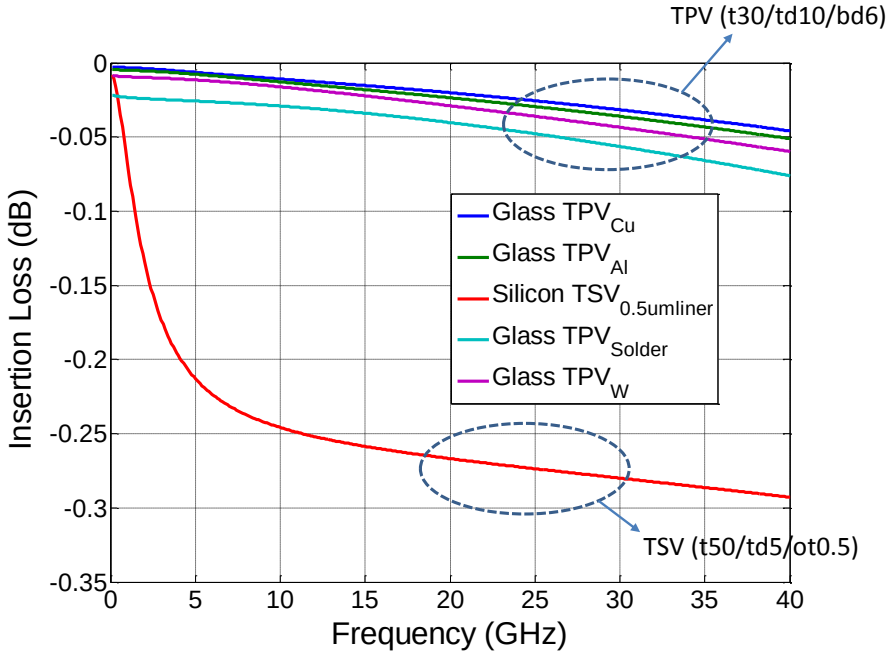
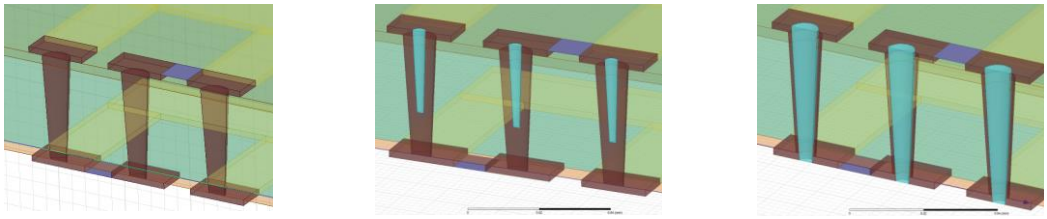


Figure 22: Insertion loss comparison of TPV in glass with different conductor materials versus TSV with copper.

d) Metallization thickness and plating thickness variations

The simulation results from the previous section revealed that copper is a good candidate to metallize TPVs in glass. The thickness of plated copper can be varied

depending on the processing time. To study the effect of variation in plating metallization thickness on insertion loss, TPVs in glass were modeled with three different metallization configurations: a) fully filled, b) semi-filled, and c) conformal with 1µm copper thickness as illustrated in Figure 23.



(a) (b) (c)

Figure 23: Schematic of the three metallization schemes, a) Fully filled, b) Semi-filled, and c) Conformal.

The semi-filled configuration is obtained as a result of the taper associated with the TPVs. The taper results in closure of via on the exit side (smaller diameter) and conformal plating on the entrance side (larger diameter). This unique configuration can be utilized to achieve stacked micro-vias in build-up or redistribution layers (RDLs) on the exit side of the TPV, while staggered micro-vias can be used on the entrance side [94]. The ability to stack micro-vias on the exit side enables higher routing density on one side of the interposer.

The insertion loss plots for the three different metallization schemes, obtained from simulations are shown in Figure 24. The responses were observed to be almost identical through 40GHz. At lower frequencies, the conformal via exhibits higher loss due to the high resistance of the thin copper metallization.

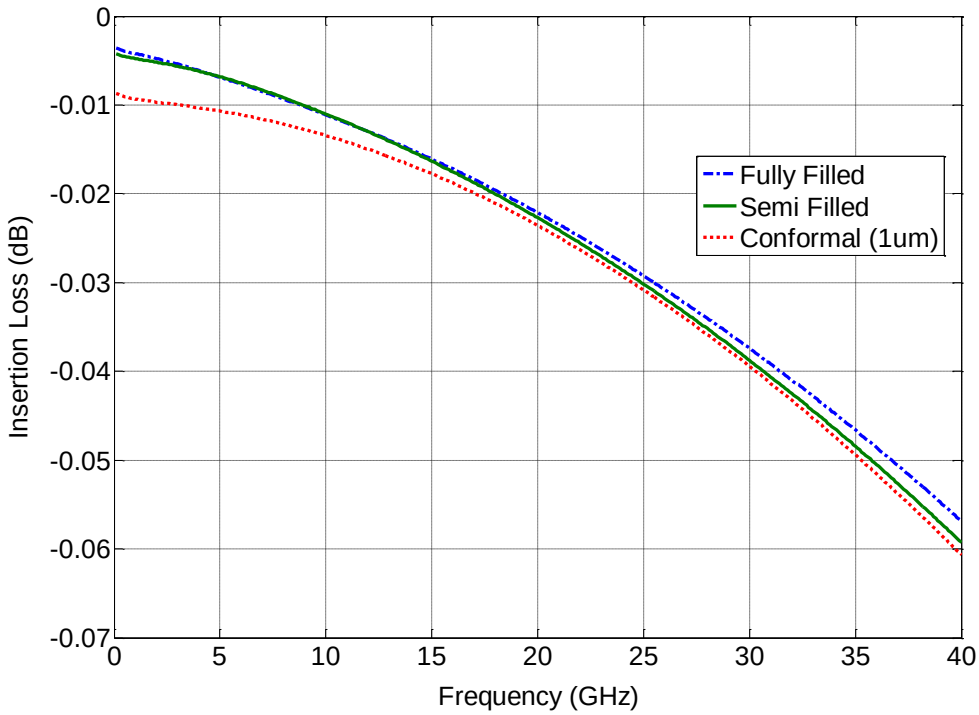


Figure 24: Insertion loss plot for TPVs with different metallization schemes.

3.3 Design guidelines for TPV formation and metallization

The study on electrical modeling and design of TPVs in glass led to several process guidelines for TPV formation and metallization. In this section, the guidelines for fabrication are outlined.

- The electrical modeling and simulation study of ultra-small TPVs in glass suggests that TPVs in glass exhibit significantly lower insertion loss and cross-talk compared to TSVs in silicon. Thus, TPVs in glass can be used for transmitting signals at high speed for digital and RF applications. The effect of via taper on TPV insertion loss was studied and it was observed that the taper did not significantly affect the signal performance.
- The change in glass material type does not significantly affect the electrical behavior of TPVs because most of the glass substrates exhibit similar values of

loss tangent and dielectric constant. The high resistivity of glass plays a significant role in achieving low insertion loss.

- The change in metallization material showed variation in insertion loss, which was attributed to the change in conductivity of the material. Copper is highly preferred as the metallization material due to its high electrical conductivity. However, there exists a CTE mismatch between copper and glass that needs to be addressed to achieve good thermo-mechanically reliability. It is important to note that the CTE of glass can be tailored to a value between 3ppm-10ppm, which is not possible in the case of silicon or organic substrates.
- The change in metallization thickness of copper did not significantly change the electrical behavior of TPVs. Hence, copper thickness can be varied (1-10µm) to optimize the thermo-mechanical stress within the TPVs.

Chapter 4

TPV HOLE FORMATION IN ULTRA-THIN GLASS

This chapter presents the materials and processes to form ultra-small TPVs in thin glass substrates, based on the design guidelines established through modeling in Chapter 3.

The primary barrier for glass interposers is the defect-free formation of ultra-small vias at close proximity to each other. Since glass is a brittle material, defects created during via hole formation can lead to reliability failures in the presence of tensile stresses in glass. The relationship between the defect size and stress required to cause failure in glass is defined by the Griffith's equation, shown graphically in Figure 25. The critical stress value, above which failures occur in glass due to crack growth decreases exponentially with increasing defect size, and high risk of failure exists even in the presence of small defect sizes (as small as 0.5µm).

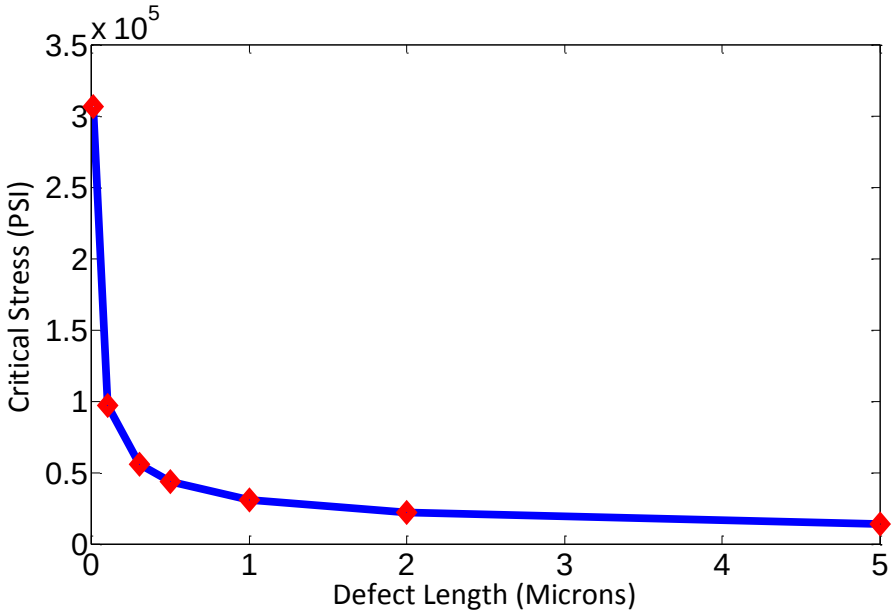


Figure 25: Graphical representation of Griffith's equation showing low critical stress values even at 0.5µm defect length.

Since the objective of this thesis is to achieve small TPVs with minimum surface damage, this chapter initially presents the theory of glass machining and the exploration of different micromachining methods. Based on this initial exploration, laser ablation was studied in further detail to achieve small TPVs with minimum surface defects. The results of excimer laser ablation in ultra-thin glass substrates and their throughput capabilities will be discussed in detail in the subsequent sections, along with the characterization of the fabricated TPVs in ultra-thin glass.

4.1 Theory and Exploration of Glass Machining Methods

Glass is an amorphous solid made up of a combination of network formers and network modifier molecules. The concentration of formers and modifier molecules can be modified to achieve the desired glass type. Some of the commonly available glass types are borosilicates, boro-alumino-silicates, and soda-lime glass. Pure quartz is comprised entirely of SiO_2 molecules and thus has a very high binding energy due to the stable nature of the tetrahedron structure of silica. On the other hand, the addition of network modifiers like alkali ions disrupts the orderly arrangement of the oxygen chain within glass and causes the effective band gap to be significantly lower compared to quartz [95]. Thus, the etch rates in glass is highly dependent on the specific composition of glass.

To successfully micro-machine any glass type, it is imperative to overcome the binding energy through physical, chemical or thermal interactions. Several mechanisms can be used to achieve through-vias in glass substrates: wet etching, dry etching, mechanical drilling, photo-structuring and laser ablation. High aspect ratio and vertical through via holes require an anisotropic etching process to minimize the lateral etching that limits the reduction of via diameter and pitch. In the following section, the fundamental theory behind each of the aforementioned glass machining

methods will be discussed, and a rationale for the selection of appropriate mechanisms for achieving the target TPV dimensions (10µm diameter at 30µm pitch) is presented.

a) Wet chemical etching

Glass is chemically inert and does not easily react with most chemical solutions. However, glass does react with hydrofluoric acid (HF), and the equations governing the etching process are summarized below:

$$SiO_2 + 4HF \rightarrow SiF_4 + 2H_2O \quad (2)$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \quad (3)$$

As the equations indicate, initially, the HF molecules react with silicon dioxide to form silicon tetra fluoride. In a subsequent reaction, the silicon tetra fluoride molecules react with HF to form H_2SiF_6, which is insoluble in HF solution.

Although wet etching process is scalable to large substrate sizes, the rate of glass removal is low (< 10µm/min) and requires masking layers to achieve the desired selectivity [96]. Additionally, the amorphous nature of glass results in isotropic etching that limits the aspect ratio. The aspect ratios targeted in this research are 3:1 or higher, and these are fundamentally difficult to achieve using pure wet etching chemistries. Therefore, this method was not explored for glass interposer applications. However, in this study, wet etching was used in combination with other process steps that resulted in a more anisotropic etch profile, such as in photo-structured glass. Additionally, as the previously discussed literature has indicated, laser assisted wet etching could be used to improve the aspect ratio.

b) Dry Etching

In the case of dry etching, the mechanism for glass removal can be physical, chemical or a combination of both. Reactive ion etching using SF_6 or C_4F_8 gases are commonly used to achieve anisotropic etching in glass.

Although dry etching methods could help achieve small diameter TPVs in glass, the process is slow with maximum reported etch rates of about 10-500nm/min [33]. Dry etching also requires a number of additional processes to form etch masks on the surface of the glass using metal deposition, lithography and etching. However, dry etching is a parallel process, wherein thousands of TPVs could be formed simultaneously. In addition, the use of thin glass substrates (30-50µm) could potentially reduce the overall etching time of TPVs. Although dry etching of glass was not explored in detail in this research, a comparison of TPV throughput for dry etching and laser ablation in ultra-thin glass is briefly discussed towards the end of this chapter.

c) Mechanical drilling

The brittleness of glass substrates poses significant challenges in through-hole formation using conventional mechanical drilling methods. Therefore, a novel method developed by Technisco (Japan) was used to explore via formation in thin glass substrates. Borosilicate glass substrates having a thickness of 200µm were used for the experiments. The dimensions of the glass samples were 2.7” x 2.7” and the design consisted of different via diameters ranging from 100µm to 250µm. The TPV pitch was kept constant at 375µm. After via formation, the sample was subjected to ultra-sonic cleaning, to remove debris from the glass surface. A top view optical image of TPVs formed using such mechanical process is shown in Figure 26. The process yielded through holes without significant cracking on the glass surface. A further

optimization of the process parameters limited the minimum defect size to about 5µm. However, this defect size is larger than the critical size that can cause reliability failures. In addition, a SEM observation was carried out to investigate the side-wall surface after TPV processing. The resulting SEM image in Figure 27 shows the small micro-chipping that occurred along the via hole edges in addition to a rough side-wall surface.

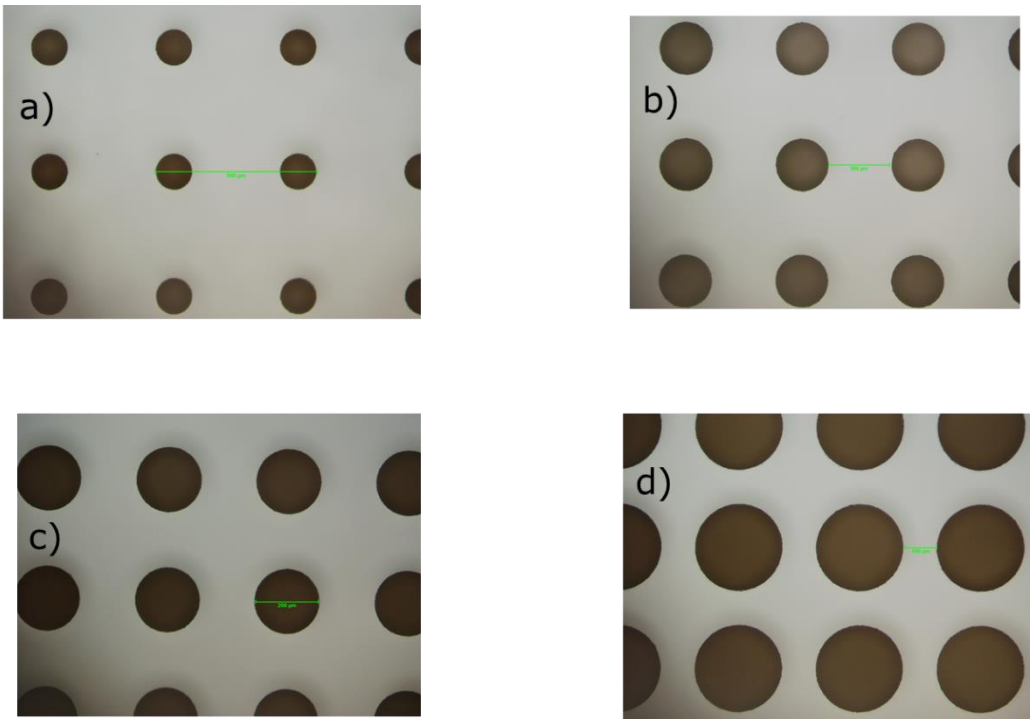


Figure 26: Optical images of TPVs formed using mechanical process: a) 100µm diameter b) 150µm diameter c) 200µm dia. d) 250µm diameter.

A cross-section analysis was performed on the TPV arrays, which revealed a vertical side-wall profile with a near 90 degree wall angle (Figure 28). The formation of through via holes having a diameter less than 100µm was observed to be difficult due to challenges associated with the mechanical process, such as machining tools, wear and breakage of tools and damage to glass.

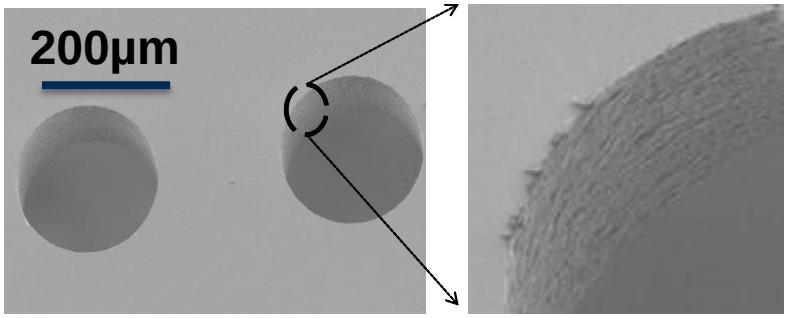


Figure 27: SEM of mechanically processed TPVs at 200µm diameter.

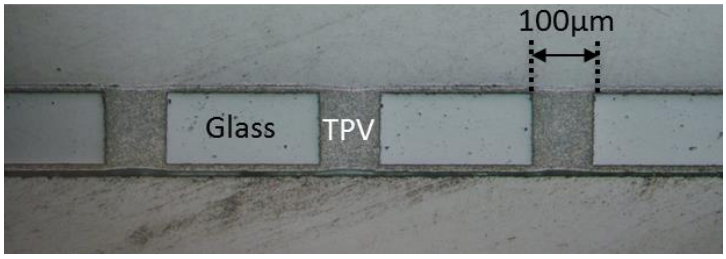


Figure 28: Optical Cross-section image of mechanically processed TPVs.

d) Photo-sensitive glass

To create photo-sensitive glass, the glass melt is carefully prepared to ensure the appropriate concentration of Ce^{+3} and Ag^{+} dopants. The TPV formation process in photo-sensitive glass consists of three steps: a) UV exposure, b) high temperature bake, and c) selective HF etching. During the UV exposure step, the valency of Ce changes from three to four, and the additional electron released during this process reduces the silver ions (Ag^{+}) to silver atoms (Ag). The reactions are summarized below:

$$Ce^{3+} \rightarrow Ce^{4+} + e^{-} \quad (4)$$

$$Ag^{+} + e^{-} \rightarrow Ag \quad (5)$$

The sample after UV treatment is then baked at high temperatures (350-450^{o}C) for few hours, during which the exposed areas are crystallized. Subsequently, a diluted HF solution is used to selectively etch away the crystallized regions,

resulting in TPVs in glass. A schematic process flow of via hole formation in glass by photo structuring is illustrated in Figure 29.

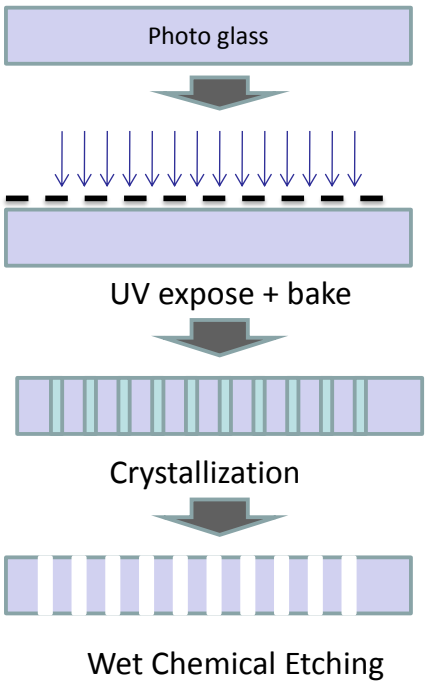


Figure 29: Schematic process flow to form vias in photosensitive glass.

Due to the fact that the process for TPV formation in photo-sensitive glass results in anisotropic etching with a high aspect ratio capability, this method was explored for small TPV formation.

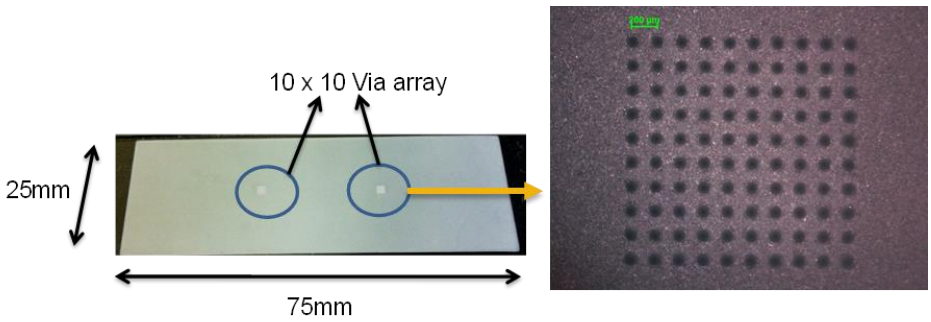


Figure 30: Snapshot image of TPV arrays formed in photo-sensitive glass substrates.

TPVs were formed in photo-glass samples, in partnership with 3D Glass Solutions Inc., using the process steps illustrated in Figure 29 [97]. The measured

TPV diameter was 100µm, and the thickness of the glass substrate was 330µm. A cross-section image of TPVs formed in photo-sensitive glass is shown in Figure 31.

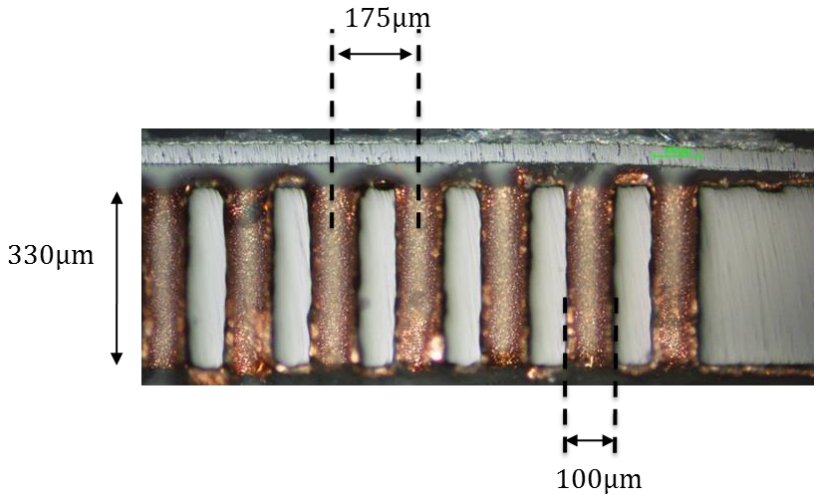


Figure 31: Cross-section image of TPVs formed in photo-sensitive glass substrates, showing high degree of anisotropy.

Photo-glass substrates require a modified chemical composition compared to normal borosilicate glass. The use of additives such as silver (Ag), cerium (Ce^{+3}) and lithium (Li) increases the melt viscosity, thus limiting the minimum glass thickness that can be achieved without grinding and polishing, to greater than 100µm.

Although prior studies have explored other glass machining methods for example, sandblasting, ultra-sonic, and water jet assisted etching; the size of the through holes achieved are significantly larger (> 100µm). Therefore, the above methods were not investigated in this research.

Based on the initial exploration of TPV formation methods, it was observed that wet etching, mechanical or photo-glass processes are not scalable to ultra-thin and large panel glass substrates and face challenges in achieving small TPV diameter (< 50µm). In the next section of this chapter, the theory and exploration of laser ablation methods for achieving smaller TPV diameters are discussed.

4.2 Theory and Exploration of Laser ablation methods

The absorption of light is dependent on the property of a medium and can be defined by Beer-Lambert's law that relates the transmitted light through a medium to the absorption coefficient and the penetration depth.

$$\frac{I}{I_o} = e^{-\alpha l} \tag{6}$$

Wherein, I/I_o = Transmitted light; α = absorption coefficient; and l = penetration depth

Glass is highly transparent in the visible region, but it can absorb light of certain wavelengths. Maximum absorption of light occurs when light is in the deep UV (< 266µm) or infrared (> 9µm) wavelengths as shown in Figure 32.

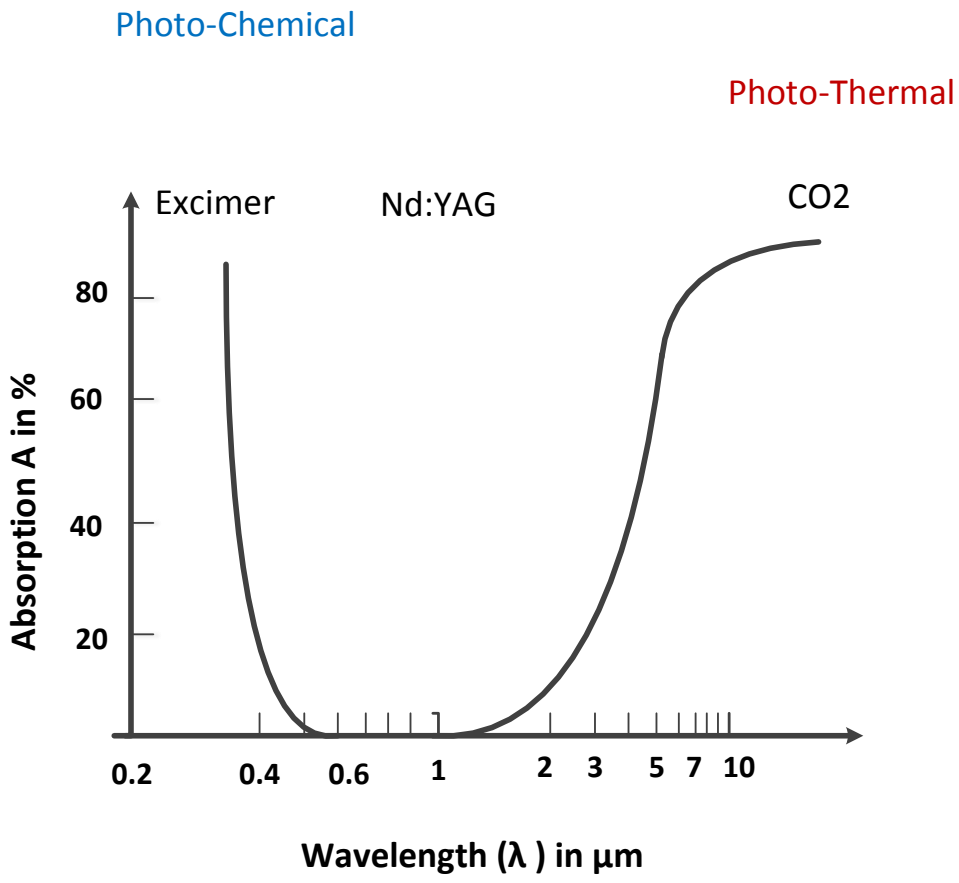


Figure 32: Absorption spectrum of glass as a function of wavelength. redrawn from [98].

The theory of laser material interaction is explained below based on [99]. Laser-glass interaction is highly dependent on the wavelength of incident light and its frequency and fluence. The work function of a typical borosilicate glass is approximately 5eV. This defines the amount of energy required to break the chemical bonds within the glass matrix. Based on the equation of energy of a photon, $E = h\nu$, (where E is the photon energy, h is the planks constant and ν is the frequency); the photon energy corresponding to a given wavelength can be computed using the formula $E = \frac{hc}{\lambda}$. It can be observed that higher wavelength lasers, operating in the infrared region (CO_2), have lower photon energy (< 1eV) compared to UV lasers, operating below 266nm (4eV-6eV). The photon energy at higher wavelengths is not sufficient to break the chemical bonds within the glass matrix. However, the higher absorption of glass leads to the transfer of photon energy (of the incident light) to vibrational energy of the atoms (within the glass matrix). This causes the laser to locally melt and vaporize the material, resulting in thermal ablation. In the case of UV lasers which operate in the excimer region (< 248nm), the energy of the incident photon causes breaking of chemical bonds within the glass matrix that results in minimum thermal damage around the periphery of the machined surface.

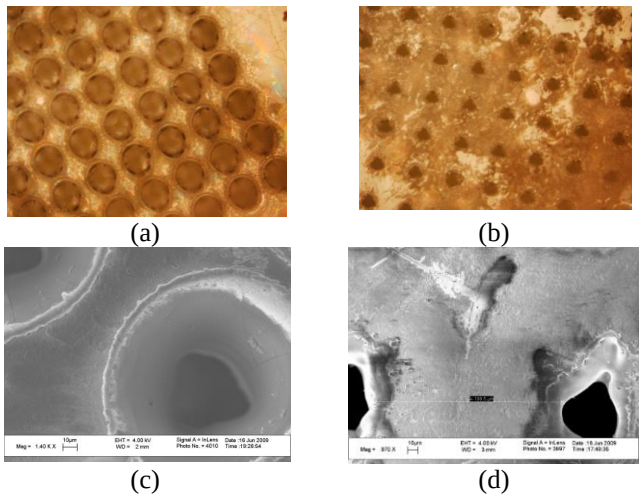
In addition to UV and infrared wavelengths, lasers operating in the visible region (300-1200nm), can also be used for glass ablation. Such lasers deliver ultra-short pulses (femtosecond or picosecond) with high peak-power, and ablation is caused by multi-photon initiated avalanche ionization [38, 100].

4.2.1 CO_2 laser ablation

For initial exploration, borosilicate glass (BSG) samples having a thickness of 175µm were subjected to CO_2 laser ablation. Large via diameters (125µm diameter at the entrance) were obtained with tapered TPV side-wall and micro-cracks were

observed along via edges. As discussed in the previous section, the ablation mechanism involves heating of the glass substrate due to atomic vibrations. Additionally, since the thermal conductivity of glass is very low (1 W/mK), the heat generated during the ablation process creates localized thermal stresses in glass, leading to cracks along via edges.

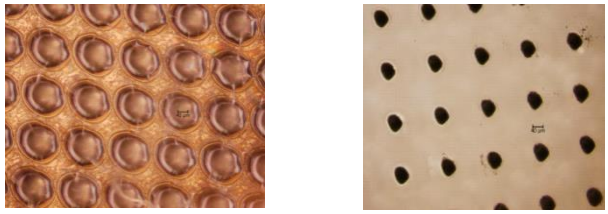
Optical and SEM images of TPV arrays ablated using CO_2 laser are shown in Figure 33. The measured TPV diameters on the entrance and exit side were 125µm and 50µm respectively. Micro-cracks were minimized by using a transverse-excited-atmosphere (TEA) CO_2 laser with short pulse duration for drilling at a slightly larger pitch (250µm), which resulted in fewer defects and minimized glass cracking (Figure 34). In comparison to continuous wave operation (CW), the use of ultra-short pulses reduces the amount of heat generated at the glass surface. The reduction in thermal energy is due to the shorter interaction time between laser and glass, and the thermal relaxation between successive pulses. However, the thermal effects cannot be completely ignored and the localized heating of glass leading to micro-crack formation is a barrier to the reduction of via diameter and pitch using CO_2 laser ablation.



(a) (b)

(c) (d)

Figure 33: SEM image of via using CO_2 laser ablation in borosilicate glass (BSG): (a), (b) Optical image of via entrance and exit; (c), (d) SEM image of via entrance and exit.

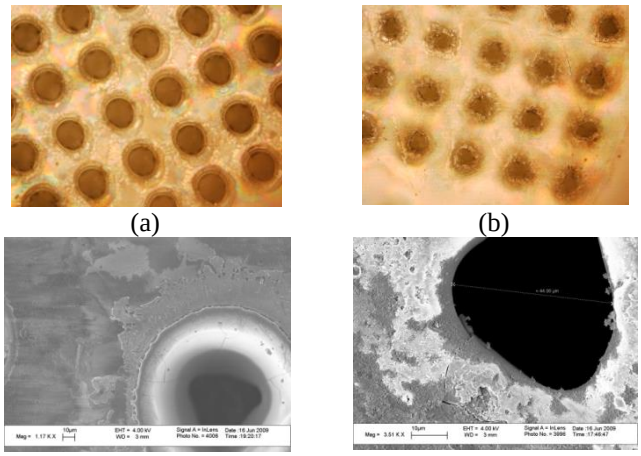


(a) (b)

Figure 34: Optical image of an array of TPVs formed using T-CO2 laser: a) entrance side and b) exit side.

4.2.2 UV laser ablation

To achieve smaller-pitch vias, UV laser ablation at a wavelength of 266nm was explored. The results obtained were comparable to that with CO_2 lasers. The TPV pitch achieved was 250µm, with entrance and exit diameters of 100µm and 50µm, respectively. In comparison to CO_2 laser, UV lasers induce less thermal damage, since the ablation is based on a combination of thermal ablation, and breaking of chemical bonds within the glass matrix (Figure 35). However, there are practical considerations for achieving smaller TPV diameters with UV lasers as reported in [101]: a) availability of high power UV lasers at lower wavelengths, b) difficulty in achieving smaller spot size and c) the lower absorption of glass in the UV-visible range.



(a) (b)

(c) (d)

Figure 35: SEM image of vias formed by 266nm UV laser: (a), (b) Optical image of via entrance and exit formed by 266nm UV laser ablation; (c), (d) SEM image of via entrance and exit.

4.2.3 Pico-second laser ablation

In addition to UV and CO_2 lasers, picosecond lasers were explored for TPV formation. The operation parameters were as follows: wavelength: 355nm; repetition rate: 61 KHz; pulse energy: 10µJ. The nonlinear absorption characteristics resulted in glass ablation with an entrance diameter of 25µm, and 2µm exit diameter, in 180µm thin glass.

(a) (b)

Figure 36: Optical image of TPVs formed using femto-second laser: a) 50µm entrance diameter and b) 12µm exit diameter

(a) (b)

Figure 37: Optical image of TPVs formed using femto-second laser: a) 25µm entrance diameter and b) 2µm exit diameter

A cross-section of TPVs ablated using picosecond lasers is shown in Figure 38.

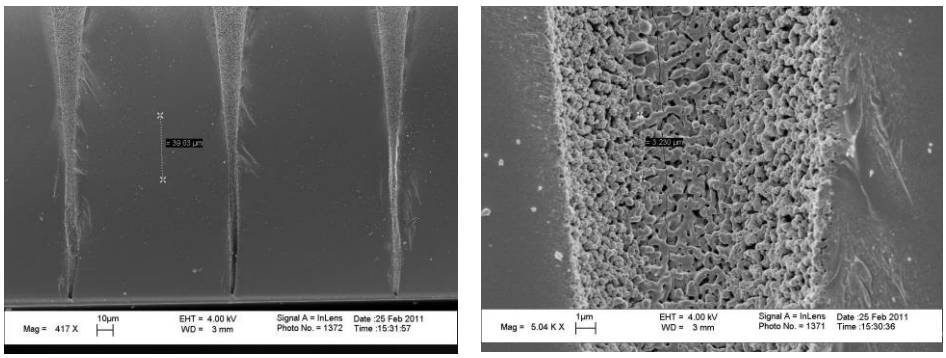


Figure 38: SEM image of TPV ablated using 355nm pico-second laser.

A highly textured side-wall profile was observed, due to localized melting and re-deposition of ablated material. Such a textured side-wall profile was observed to be consistent with some of the prior studies using short-pulse duration lasers on glass [37]. Although small TPV diameters were achieved using picosecond laser ablation, the size of defects created were fairly large (~0.5µm) which could eventually lead to glass cracking during subsequent handling and metallization processes. Moreover, the etch rate in glass was observed to be very slow (2-3 seconds per via). Due to the aforementioned reasons pico-second laser ablation was not pursued further for ultra-thin glass TPV formation.

4.2.4 Excimer laser ablation

As described in the earlier section, the absorption coefficient of glass increases with decrease in wavelength. Since glass has high absorption at 193nm, almost 95% of the laser energy is utilized to break the chemical bonds within the glass matrix. A small part of the laser fluence is converted into heat energy, which is negligible, and thus the thermal stresses are also minimal. Both 248nm-KrF and 193nm-ArF lasers were explored for small TPV hole formation in glass. A cross-section image of TPV formed using KrF laser is shown in Figure 39. The measured diameter on the entrance side of TPV was 80µm, and the thickness of the glass substrate was 180µm. A closer inspection of the side-wall of TPV revealed a textured surface with micro-roughness (Figure 39).

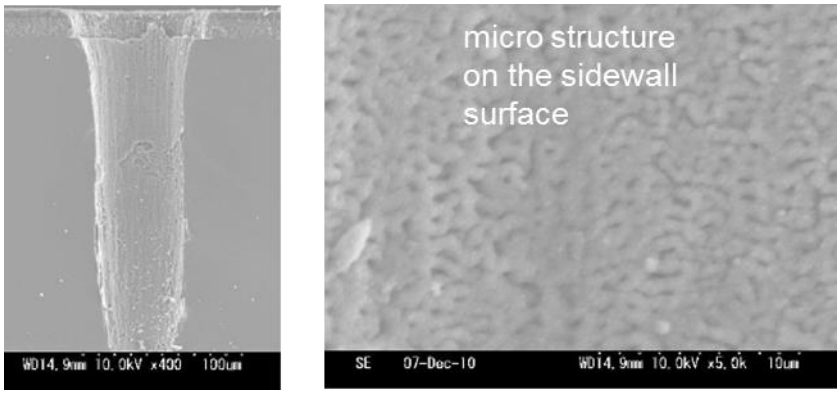


Figure 39: Cross-section SEM image of TPV formed using KrF laser.

In addition to KrF lasers, ArF based excimer laser that emits light at 193nm was used to form TPVs in glass. The energy of laser beam was 7-12mJ per pulse, with a repetition rate of 25-200Hz. The experiment resulted in TPVs with smaller diameter and pitch (50µm) compared to UV and CO_2 laser ablation in 175µm thick glass substrates. The entrance and exit diameters measured were 35µm and 22µm respectively as shown in Figure 41 and Figure 42. No micro-cracks were observed in the glass surface or on the TPV side-wall after laser ablation.

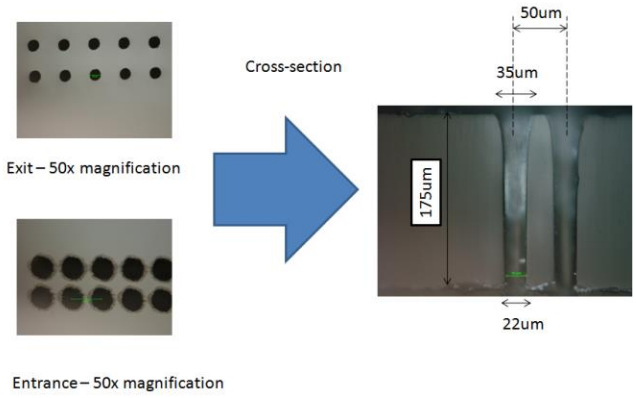
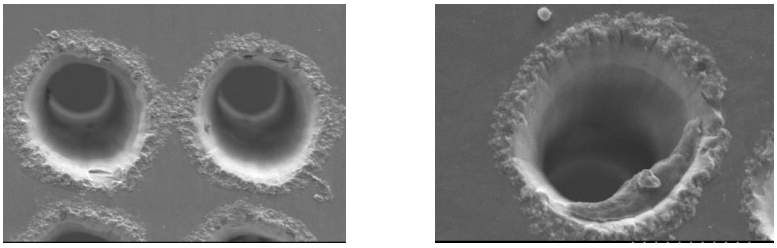


Figure 40: Small TPV hole formation in glass using 193nm excimer laser ablation.

Cross-section examination of these TPVs was conducted and the images showed a smooth via sidewall profile (Figure 42). SEM imaging was carried out to investigate the sidewall surface and the ablation debris deposited around via entrance.



(a) (b)

Figure 41: SEM images of via entrance, using excimer laser ablation at different magnifications a) 1.2K and b) 1.8K.

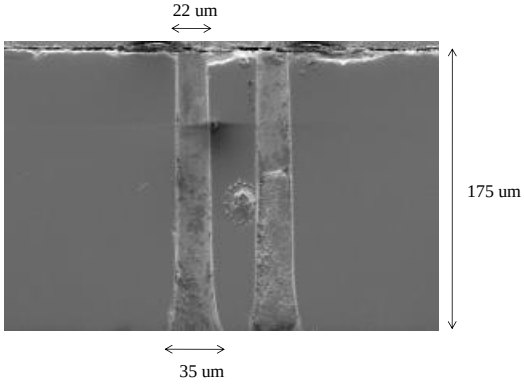


Figure 42: SEM cross-section view of 50µm pitch TPV formed using excimer laser.

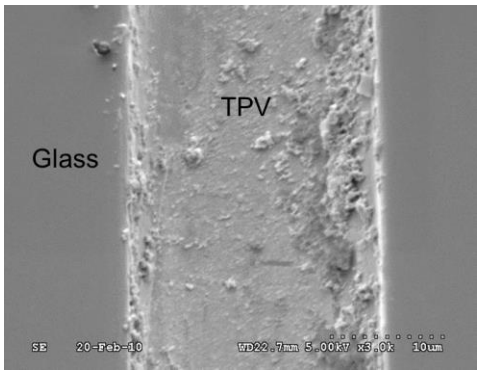


Figure 43: SEM image of TPV cross-section.

The residue observed inside the TPV in Figure 43 can be attributed to the alumina particles used for polishing to obtain the cross-section image. In addition, the molten glass from the ablation process was observed to have re-deposited on the surface near the entrance side of the TPVs. This debris formed on the glass surface causes surface irregularities that can create a significant challenge in subsequent

lithography processes. A SEM image of TPV showing re-deposited glass is shown in Figure 44.

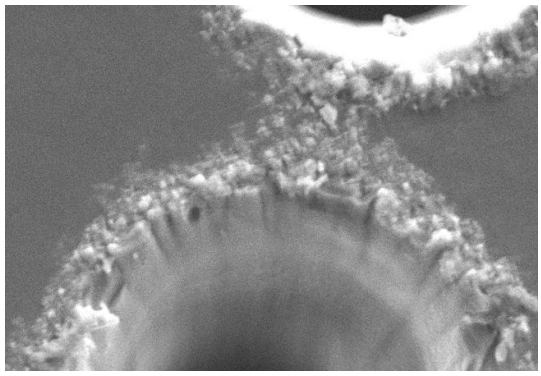


Figure 44: SEM image of TPV showing re-deposited glass after excimer laser ablation.

One of the methods to remove this residue is to chemically etch the re-deposited glass using a buffered HF solution. Wet chemical etching helps in two ways: a) removes the re-deposited glass on the glass surface and b) helps in rounding of surface and edge defects, thereby increasing the fracture toughness of glass with vias [102].

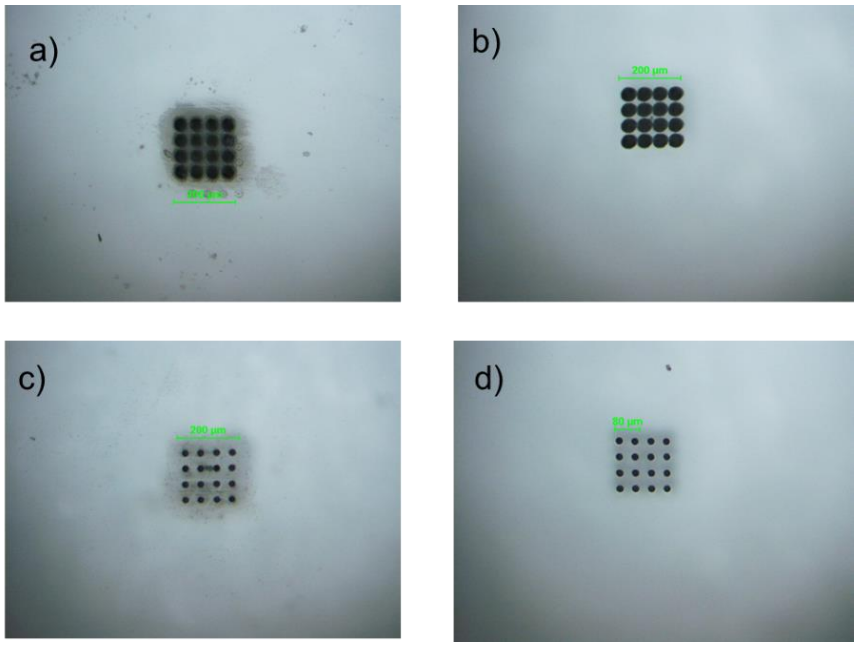


Figure 45: Optical image of TPV array formed using ArF laser ablation: a) entrance side after ablation, b) entrance side after treatment with buffered HF for 9mins, c) exit side after ablation, d) exit side after treatment with buffered HF for 9mins.

A SEM observation of the TPV array was carried out before and after buffered HF treatment and the images obtained are shown in Figure 46.

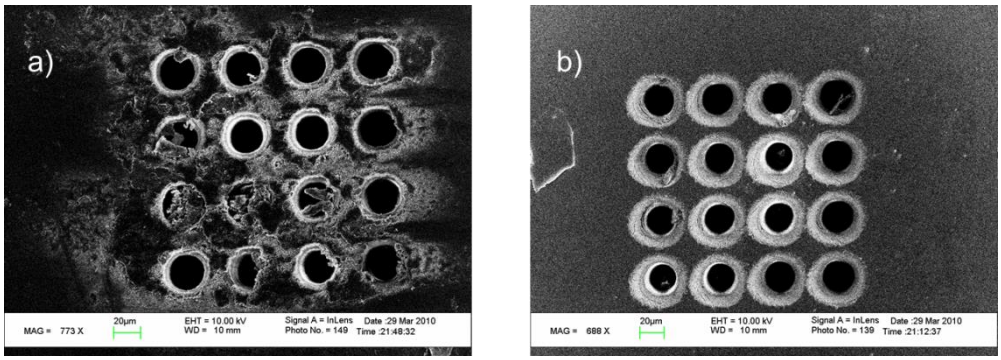


Figure 46: SEM image of TPV array: a) after ablation showing debris formation and b) after treatment with buffered HF solution.

4.3 Novel 'polymer on glass' approach prior to TPV formation

One of the fundamental challenges in processing glass panels to form interposers is the defect-free handling of thin glass in panel form (> 300mm x 300mm). Defects or cracks in glass can be formed very easily at different stages of processing, for example, during, a) glass manufacturing, b) handling during processing, c) formation of small TPVs, and d) interposer fabrication.

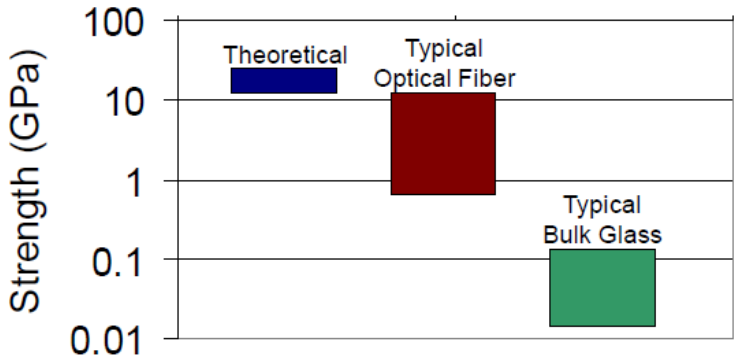


Figure 47: Strength of glass substrates from pristine surfaces as drawn, and as exposed to ambient [53].

Glass is a brittle material. Although the theoretical strength of glass is extremely high as shown in Figure 47, defects are created during subsequent handling steps which significantly reduce its fracture toughness. As such its strength is higher

in compression than in tension. Glass surfaces, therefore are less prone to failures when subjected to compressive stresses, as opposed to tensile stress. The use of surface coatings on glass, has been studied to improve the strength of glass [103], by preventing the formation of defects on the glass surface. This research explores new polymer film coatings on glass for improved handling of thin glass and for reducing the risk of glass breakage.

To improve the fracture toughness of glass interposers, a thin layer of polymer (~ 20µm), having a CTE higher than glass, is laminated on both sides of the glass substrate. Such an approach helps in four ways, a) introduces compressive stress onto glass, originating from the CTE mismatch between polymer and glass during the high temperature lamination, b) eliminates the need to directly metallize onto the glass surfaces, c) protects the glass surface from damage during laser ablation of TPVs, and d) provides a conformal coating over surface defects, thereby suppressing defect growth propagation. Figure 48 shows the cross-section schematic, comparing bare-glass approach to the proposed polymer on glass approach.

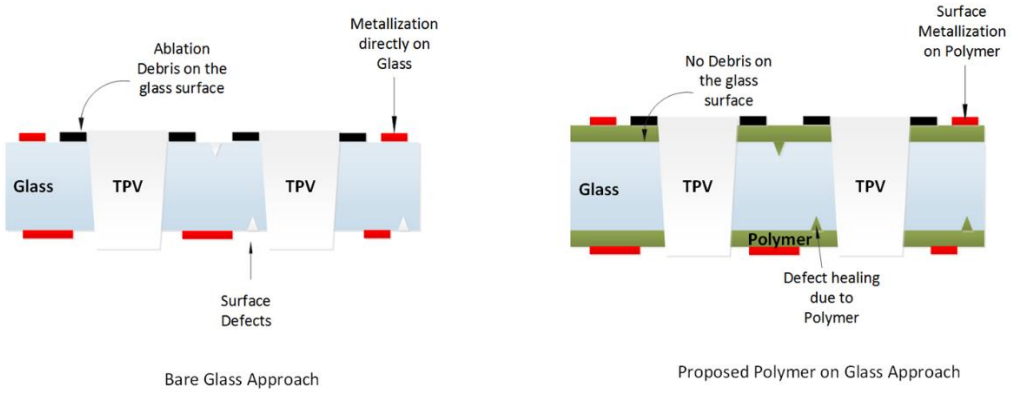


Figure 48: Comparison between bare glass approach, and the proposed polymer on glass approach.

The polymer material used in glass interposer should have the following properties, a) good adhesion to the glass surface and low moisture uptake, to prevent delamination and reliability issues, b) low loss-tangent, for superior electrical

performance, c) higher CTE than glass, to induce compressive stress on the glass surface, d) low modulus, and e) higher transition temperature (T_g), for withstanding reflow temperature during die and package assembly.

Two different polymer systems were explored for lamination onto glass; a) RXP4M from Rogers Corporation (USA) and b) Zeon-insulation-film (ZIF) from Zeon Corporation (Japan). Both polymers are available in thin and dry-film format that enables the lamination process to be easily scalable to large-panel sizes. The material properties of the two polymers are show in Table 6.

Table 6: Material properties of RXP4M and ZIF polymers

Properties	Unit	ZIF	ZIF-low loss	RXP-4M
CTE	ppm/^{0}C	25	25	45
Tg (DMA)	^{0}C	187	185	169
Dk	(1~10GHz)	3.1	3.1	2.96
Df	(1~10GHz)	0.011	0.005	0.0024
Water Absorption	%	0.3	0.1	0.138
Lamination Temperature	^{0}C	120	120	232
Youngs Modulus	GPa	6.9	7.7	-
Laser Process-able	-	Yes	Yes	Yes
Flow-ability	-	Yes	Yes	No

RXP4M exhibits a lower dielectric loss tangent value (tan δ = 0.0024) that make them suitable for high frequency RF applications. On the other hand ZIF provides an excellent smooth surface (Ra ~ 5nm) for fabricating small-line width

RDLs. These thin dry-film polymers were applied on both sides of glass prior to via hole formation. The details about the lamination process are explained in chapter 6.

4.3.1 CO_2 laser ablation in polymer laminated glass surfaces

The initial study on CO_2 laser ablation in bare glass samples revealed micro-cracking with large TPV diameters (> 100µm). To form smaller via diameter, a copper-window approach was explored in which a thin layer of copper (2-5µm) was deposited on a single side of the polymer laminated glass substrate which was lithographically patterned. The rationale behind depositing copper is twofold: a) to dissipate the heat generated during ablation in the lateral direction (XY plane) through the copper surface and b) to reduce the thermal damage on the entrance side of TPV. Copper exhibits high reflection at the CO_2 laser wavelength (10.6µm) and was thus used as the metal layer for the window approach. A schematic cross-section of the proposed approach is shown in Figure 49.

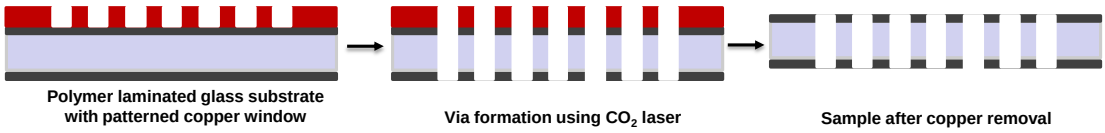


Figure 49: Schematic cross-section of copper-window approach.

The pattern consisted of circular openings that exposed the polymer surface to the incident laser beam. Subsequently, TPVs were formed through the Cu-polymer-glass stack-up, and the Cu layer was finally removed using a micro-etch solution.

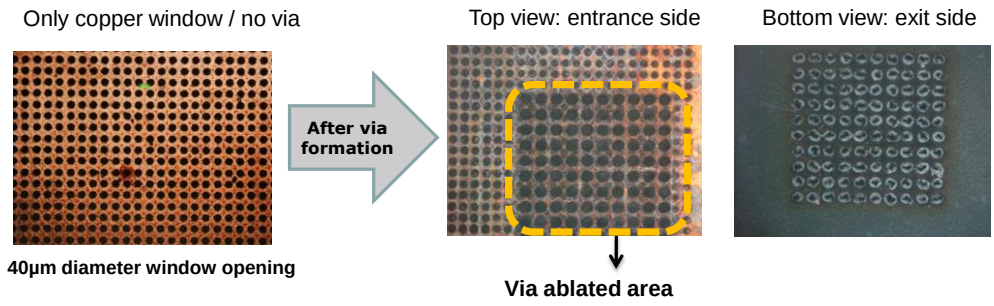


Figure 50: Optical image of TPVs in glass using the copper window approach.

The results obtained after laser ablation are shown in Figure 50. It was observed that the copper window was not effective in achieving smaller TPV diameters. This result can be attributed to the use of thin copper layers (3-5 µm) and the need for high laser fluence to drill through glass that is higher than that required to ablate polymer materials [104].

On the other hand, the implementation of CO_2 laser ablation directly on polymer laminated glass substrates resulted in excessive damage to the polymer layer especially on the entrance side of TPV as shown in Figure 52. Although the copper-window approach was not useful in achieving smaller TPVs, the use of thin Cu layers prior to ablation can minimize the extent of thermal damage caused to the polymer layers on the entrance side of the TPVs. This concept is illustrated in Figure 51. Copper was deposited on both sides of the sample to prevent warpage issues from single side deposition. Damage to the polymer on the entrance side was significantly reduced while drilling through the copper layer as shown in Figure 53.

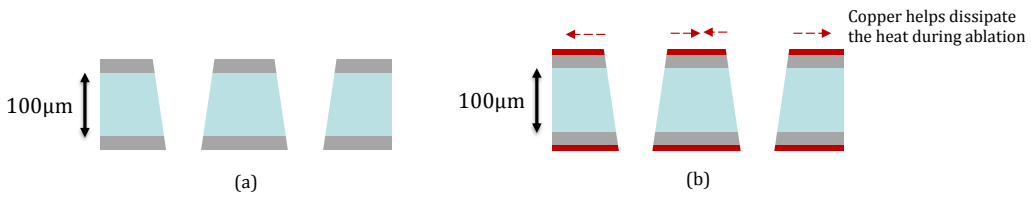


Figure 51: Schematic cross-section of CO_2 laser ablation with and without copper on the surface

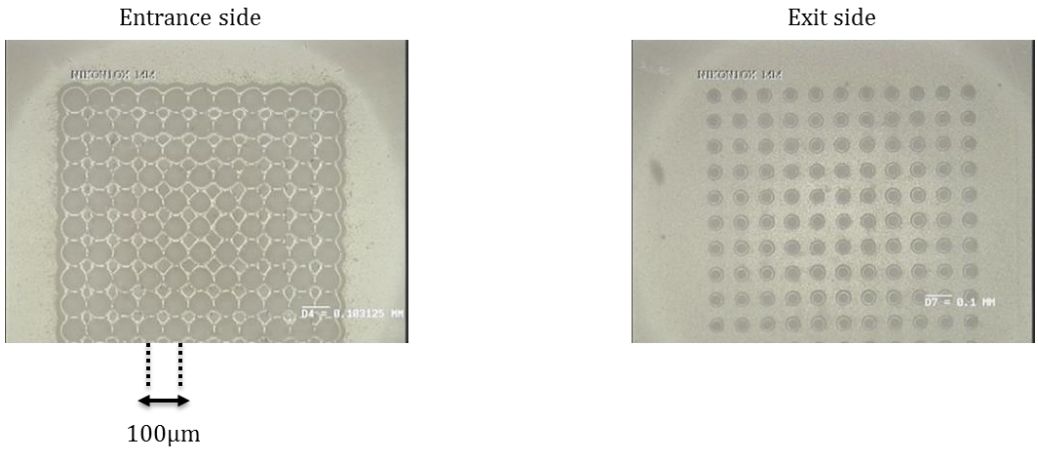


Figure 52: Optical image of TPV array formed using CO_2 laser ablation on polymer laminated glass.

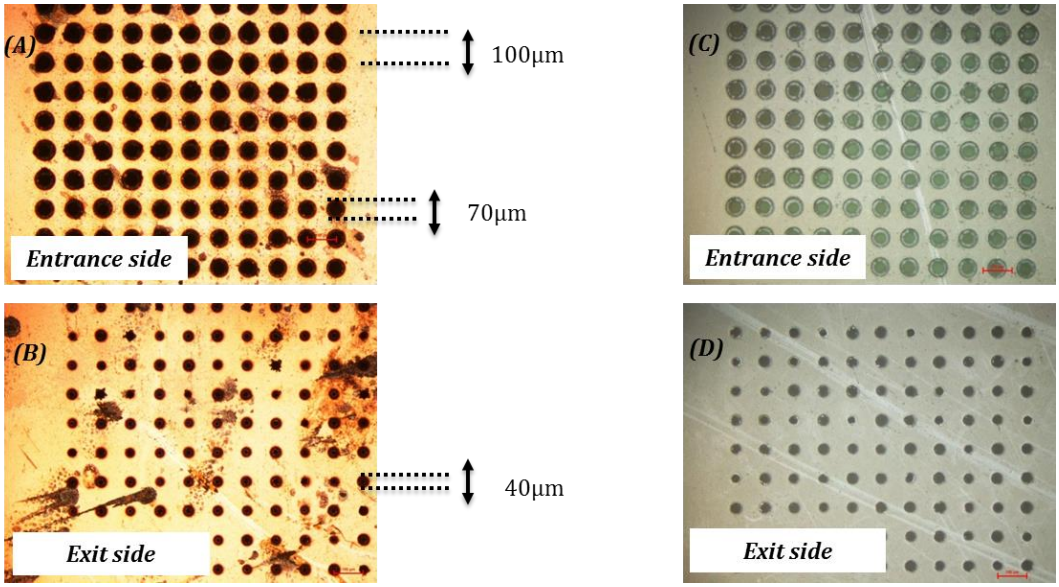


Figure 53: Optical images of TPV array formed using CO2 laser ablation: A) Entrance side before copper etching, B) Exit side before copper etching, C) Entrance side after copper removal, D) Exit side after copper removal.

4.3.2 Excimer laser ablation in polymer laminated glass surfaces

The thin film dielectrics must have high absorption at UV and excimer wavelengths to achieve efficient ablation through the glass-polymer stack-up. Figure 54 shows a cross-section image of excimer laser ablated vias in polymer-laminated glass. The laser parameters were tuned to achieve almost vertical TPV profile, with a constant via diameter of 30µm at 60µm pitch in 175µm glass thickness.

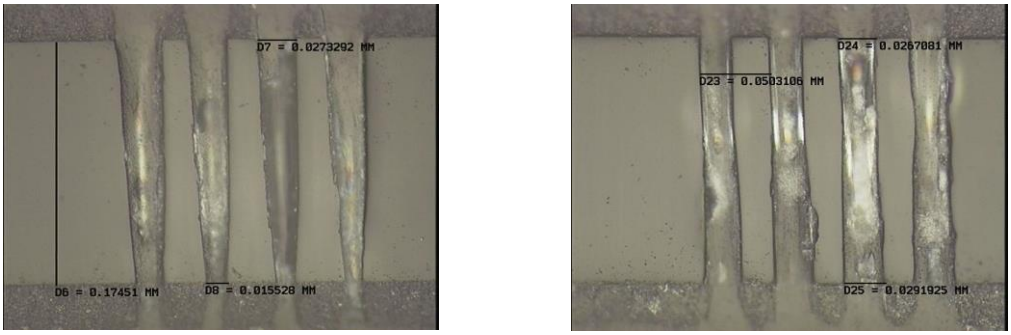


Figure 54: 193nm Excimer laser ablation on RXP4M lamination glass: a) tapered TPV sidewall profile and b) vertical TPV sidewall profile.

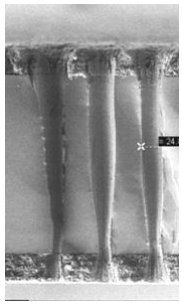
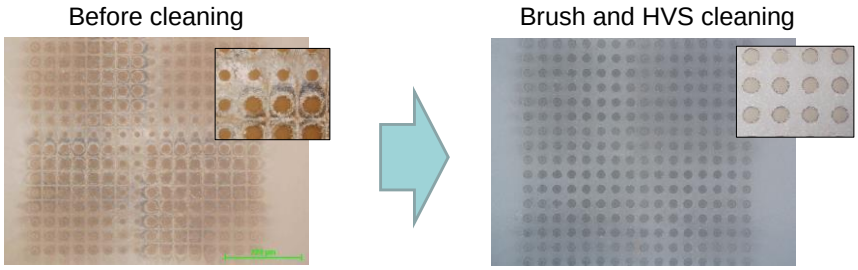
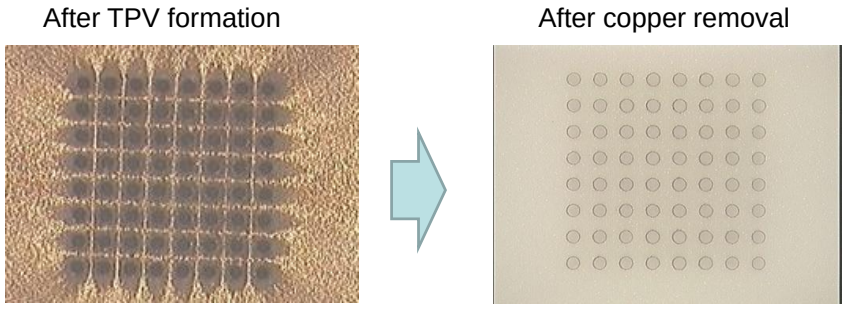


Figure 55: SEM image of cross-section of excimer via on cleaved glass sample laminated with polymer.

Laser ablation using 193nm resulted in debris on the polymer surface near the TPV entrance. This debris comprises mainly of molten glass and polymer remnants that creates a non-uniform surface and poses challenges in fabricating small-line width RDL traces around the TPVs. Two methods were explored to remove this ablated material from the polymer surface: a) use of a brush and high-velocity spray (HVS) cleaning method and b) use of a sacrificial layer prior to ablation such as copper. The results obtained using the two approaches are shown in Figure 56 (a, b).



(a)



(b)

Figure 56: Post-ablation TPV debris cleaning methods, a) mechanical, b) Cu protective film.

An array of 64 vias in eight rows and columns is shown in Figure 56. These vias were formed simultaneously (using mask projection) in 180µm thick glass substrates that were laminated with polymer (RXP4M) on both sides. The entrance and exit diameters of the TPVs measured 60µm and 35µm respectively and the TPV pitch was 120µm.

In the cleaning method illustrated in Figure 56a, a high velocity spray and brush system was used to physically remove the debris from the polymer surface. Deionized water (DI-water) was used as the solution for the spray, although other solvents could also be used for the cleaning process.

Alternately, a sacrificial layer approach can also be applied to minimize debris on the polymer surface after ablation. A thin layer of copper (1µm) was deposited on the polymer surface prior to laser ablation. The copper was subsequently etched after ablation, and the resulting polymer surface was observed to be devoid of residues as shown in Figure 56b.

Based on the study so far, it was observed that laser ablation can be a feasible method to form TPVs in glass which is laminated with a thin layer of polymer on both sides. A summary of the minimum TPV geometry that was achieved using the different laser processes is shown in Figure 58. It was observed that excimer lasers

operating at 193nm are best suited to machine small TPV holes in thin-glass, with minimum thermal damage.

Additionally, a comparison between the different laser processing methods and the resulting TPV side-wall profile was studied through SEM observation. The images obtained are shown in Figure 57. It was observed that the TPV processing using CO_2 and UV lasers results in micro-cracking along the side-wall due to the thermal nature of the ablation process. On the other hand, although pic-second laser ablation resulted in smaller TPV diameters, the resulting side-wall surface was observed to the highly textured with surface roughness values in the range of 0.5-1µm. Excimer laser ablation using 193nm ArF lasers, resulted in smooth TPV side-wall profile and smooth interface with minimum defects.

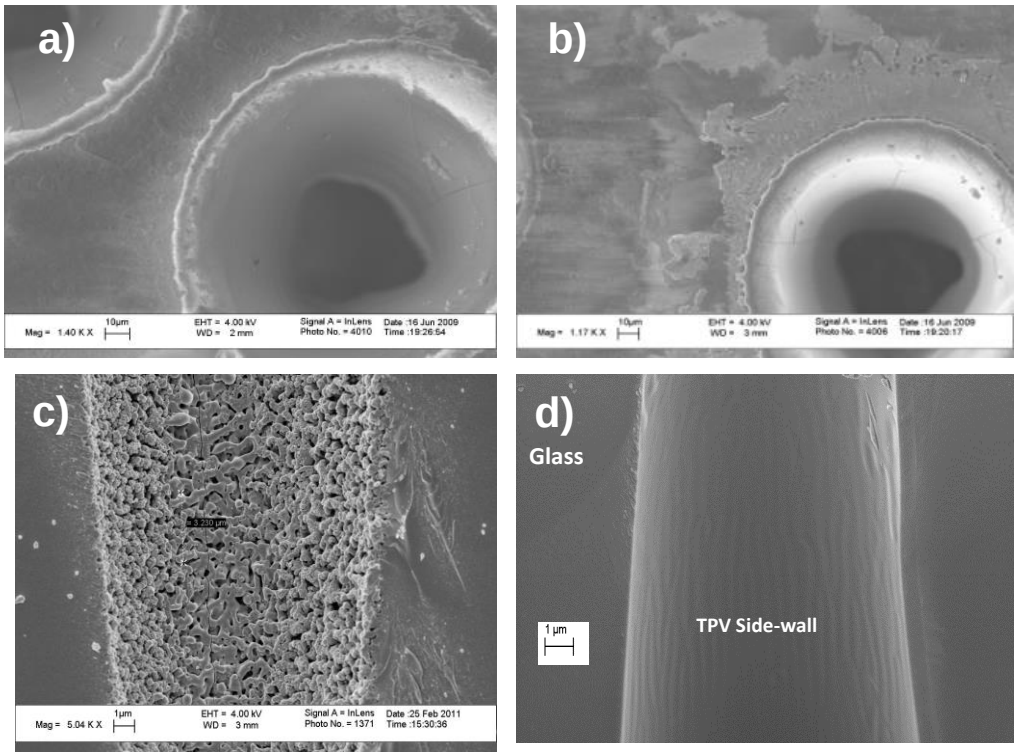


Figure 57: TPV side-wall profile after laser ablation: a) CO_2 laser showing micro-cracks and heat-affected-zone (HAZ), b) UV laser showing micro-cracking, c) Pico-second laser, showing rough side-wall surface, and d) excimer laser ablation, showing smooth side-wall.

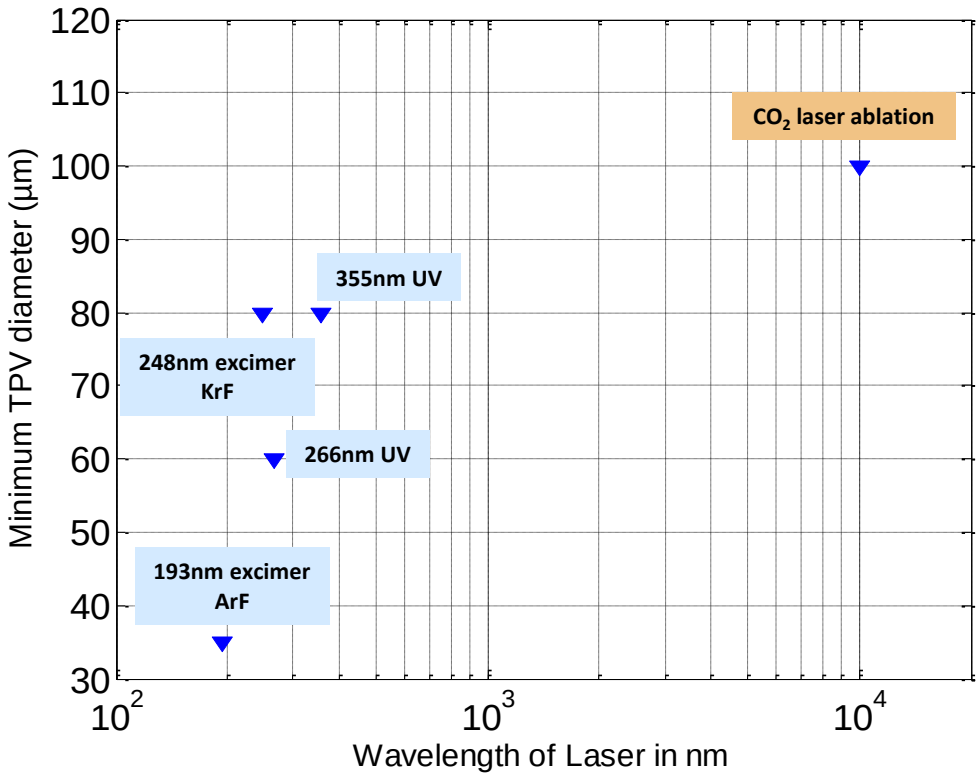


Figure 58: Minimum TPV diameter achieved in 180µm thick glass as function of different lasers.

The research results presented so far indicated that lower wavelength excimer lasers yield small TPV holes in glass substrates with minimum defects. This result was attributed to the fact that most of the incident energy (from excimer lasers) was absorbed within few micro-meters from the glass surface. This absorbed energy cause material removal through photo-chemical reactions (breaking of atomic bonds within the glass matrix), resulting in precise machining of small TPV holes with minimum thermal damage to the glass surfaces. Further, it was shown that the use of thin film polymer layers on glass could improve handling and also minimize defects on the glass surface. Based on this learning, the remaining part of this chapter will focus on excimer laser ablation in ultra-thin glass substrates (30µm).

4.4 Theory of Excimer laser ablation

An excimer laser emits radiation in the deep-UV region. Depending on the type of gas used as the lasing medium, the wavelength of the LASER falls between 157nm and 308nm. The lasing medium typically consists of a mixture of halogen (F or Cl) and inert gas (Ar, Kr or Xe). As shown in Figure 59, the lasing action involves a sequence of two steps. In the first excitation step, an electric current is passed through the gas mixture so that the inert gas combines with the halogen to form a complex molecule (e.g. ArF, KrF, XeCl). In the second step, this molecule subsequently dissociates to the ground state through stimulated or spontaneous emission of radiation. The above two steps (excitation and emission) are expressed in the form of equations as shown below. The energy-band diagram describing the lasing action is illustrated in Figure 59.

$$2\ Ar + F_2 \rightarrow 2\ ArF^*\ (\text{excited energy state}) \quad (7)$$

$$2\ ArF^* \rightarrow 2\ Ar + F_2\ (\text{ground state}) \quad (8)$$

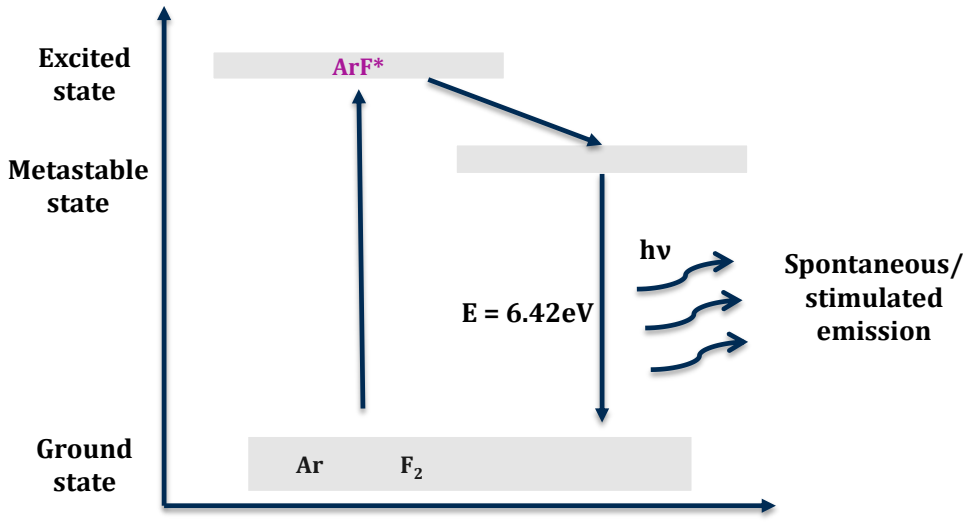


Figure 59: Energy band diagram describing excimer laser emission.

The common gas chemistries used as the lasing medium, along with their corresponding values of wavelength and energy of emitted radiation are summarized in Table 7.

Table 7: Excimer lasers: Gas chemistry, wavelength and energy

Gas chemistry	Wavelength (λ)	Energy (hν)
F_2	157 nm	7.9 eV
ArF	193 nm	6.42 eV
KrF	248 nm	5 eV
XeCl	308 nm	4.03 eV

The values of energy shown in Table 7 were computed using the formula $E=hc/\lambda$ by substituting $4.135e^{-15}$ eVsec for the plank's constant (h), and a value of $3x10^8$ m/s for the speed of light (c). It is apparent that the energies associated with the smaller wavelengths are significantly higher because of the inverse relation between energy and wavelength. Moreover at smaller wavelengths, most of the incident energy is absorbed by the glass near the surface. Thus, precise features can be easily achieved on the sample surface. Although, a very short wavelength (157 nm) would facilitate more efficient ablation of TPVs in glass, the high degree of opacity of most materials at 157 nm poses fundamental challenges to efficiently operate laser systems over longer periods of time, without damaging the optics within the laser system.

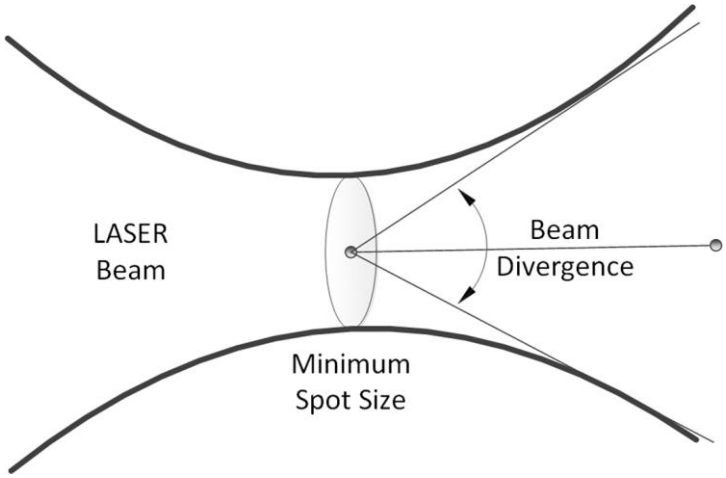


Figure 60: LASER beam spot size and beam divergence.

To form small TPVs in glass, in addition to the high energy of the laser pulse, the ability to focus the beam (typically Gaussian) to a small spot size with minimum beam divergence is critical. The diameter of the spot size is defined as the distance between the points on the Gaussian curve where the magnitude is $1/e^2$ of the maximum value. The smallest possible diameter (minimum spot size) of the laser spot is a function of the wavelength, and is mathematically expressed by the following equation:

$$d_0 = \frac{4f\lambda}{\pi D} \tag{9}$$

Where, d_0 is the minimum spot size, f is the focal length of the lens, λ is the wavelength and D is the diameter of the beam emanating from the laser. However, there are practical limitations to the minimum spot size that can be achieved due to beam divergence. Mathematically, the divergence can be expressed by the following equation:

$$\emptyset = \frac{2\lambda}{\pi w_0} \tag{10}$$

In the above equation ϕ is the beam divergence angle, λ is the wavelength, and w_0 is the minimum diameter at the waist of the beam. Similar to the equation used to compute the minimum spot size, the beam divergence is also directly proportional to

the wavelength of the laser beam, and thus a smaller wavelength leads to smaller beam divergence.

In summary, it can be observed that due to the lower wavelength of excimer lasers they can be focused to a smaller spot size on the sample with smaller divergence compared to UV or CO_2 lasers.

The formation of through vias in glass using laser ablation results in a tapered TPV profile. This taper angle is a function of process conditions and glass thickness. A simple theoretical model is presented in the following section to study and understand the relation between the TPV geometry and the glass thickness.

4.5 Theoretical model to study the process induced TPV side-wall taper as a function of glass thickness

In the previous section it was observed that TPVs formed using laser ablation show tapered side-wall profile which can be attributed to the self-focusing nature of the laser beam. A simple theoretical model was developed, to provide guidelines for selecting the desired TPV geometry and glass thickness based on given process conditions. The four important geometrical parameters that were considered are: entrance diameter of TPV (D), exit diameter of TPV (d), via taper angle (Φ) and glass thickness (t). An equation that relates these four parameters is shown in Equation 11.

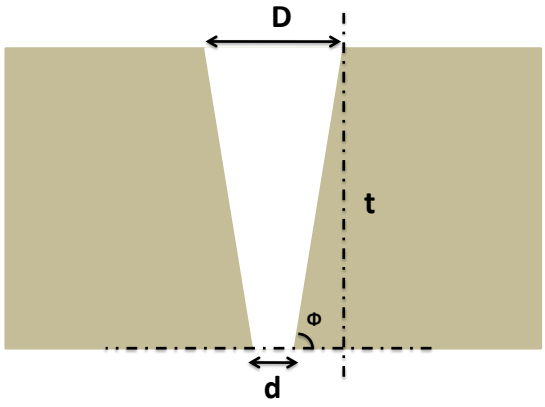


Figure 61: Schematic cross-section of glass TPV.

$$\boldsymbol{d = D - \frac{2t}{\tan \Phi}} \qquad (\mathbf{11})$$

d = Exit diameter of via

D = Entrance diameter of via

t = Substrate thickness

Φ = effective via side-wall angle

The effective via side wall angle was obtained by connecting the edges of the vias on the entrance and exit sides. Via dimensions are process-dependent (aspect ratio achievable), and the value of Φ was approximated to be independent of the exact side wall shape (Figure 61). Moreover, the smallest feature size and ablation rate of glass depends on the glass composition. From equation 11, it is evident that for Φ = 90^o (vertical via sidewall), the entrance and exit via dimensions are equal. A negative value of d indicates that via is not completely drilled through the substrate (blind-via). In Figure 62, the variation of the exit via diameter as a function of the glass substrate thickness is plotted. The side-wall angle was kept constant (Φ = 87.8^o), while the entrance diameter (D) was varied from 20µm to 150µm. The choice of angle 87.8^o was based on the laser process capability of excimer laser (based on the results shown in the previous sections). It can be seen that in order to achieve through vias having an entrance diameter of 20µm, the glass substrate thickness needs to be less than 250µm for the given process conditions (Φ = 87.8^o).

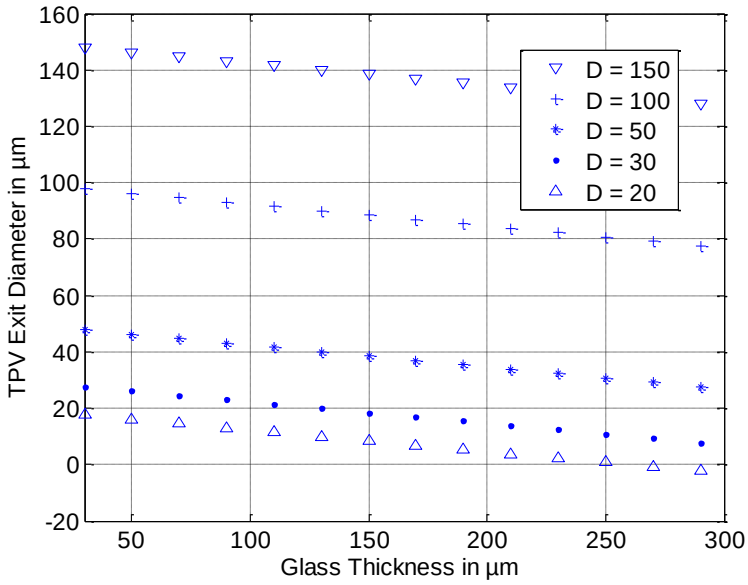


Figure 62: Exit via diameter as a function of glass thickness with fixed via side wall angle (Φ = 87.8°) and variable D.

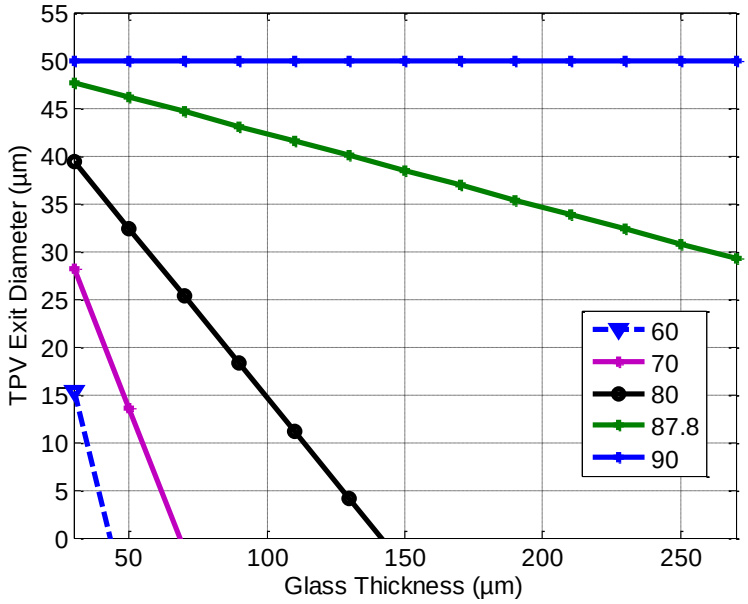


Figure 63: Exit via diameter as a function of glass thickness with fixed D (D = 50µm) and variable Φ.

Similarly, the exit via diameter was obtained as a function of glass thickness (Figure 63) by keeping the value of D constant (50µm), and varying the side wall angle Φ from 60° to 87.8°. The theoretical model provides a relation between the TPV dimensions and the glass thickness, based on the process conditions. Thus, one can

choose the appropriate process and glass thickness to meet a specific TPV geometry requirement. The model helps define design rules, based on process capability.

4.6 Effect of glass thickness variation on TPV diameter

An Argon Fluoride (ArF) based excimer laser was used for the formation of vias in glass with different thicknesses. The experimental results of via formation are summarized in Figure 64 and the measured TPV diameter and pitch as a function of glass thickness is shown in Figure 65. The experimental results indicated that smaller TPV diameters similar to dimensions in TSVs could be achieved using thinner glass substrates. An additional advantage of using thin-glass substrates is the reduced number of laser pulses required to completely etch through the substrate, which leads to shorter processing time.

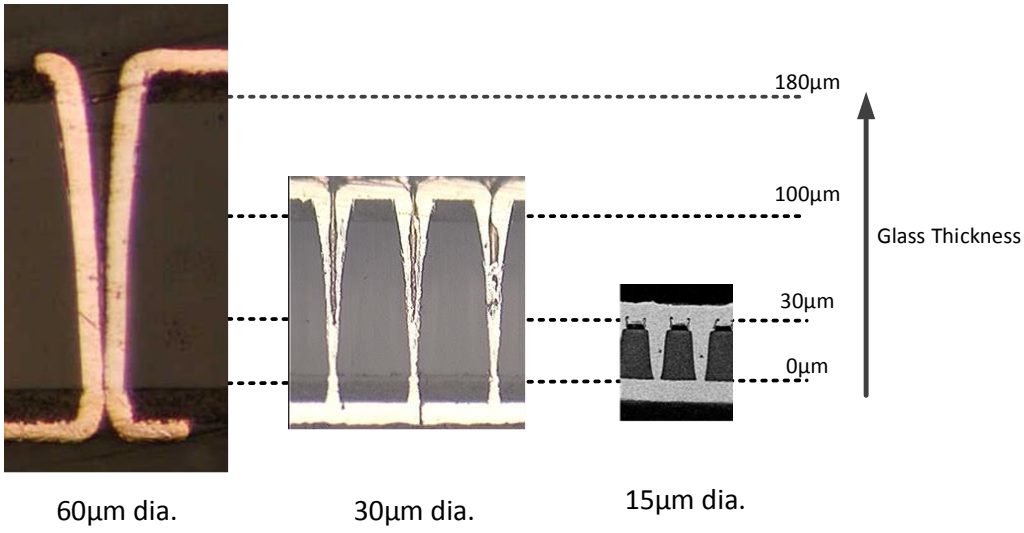


Figure 64: Cross-section image of metallized TPVs showing the TPV profiles as a function of glass thickness.

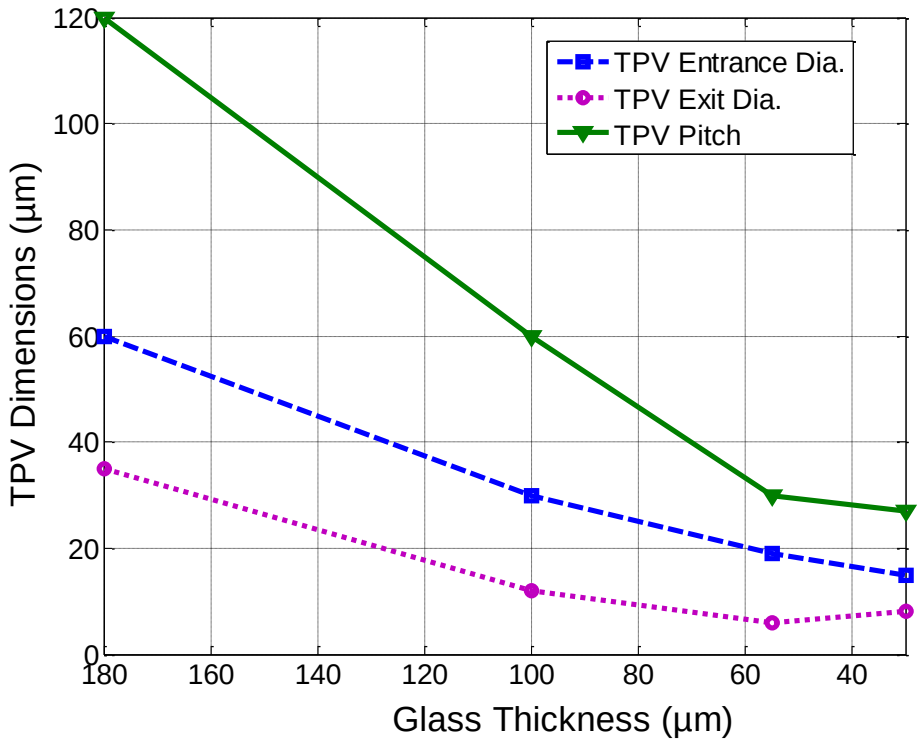


Figure 65: Measured TPV diameter and pitch as a function of glass thickness.

4.7 Excimer Laser ablation results on ultra-thin glass substrates (30-55µm)

4.7.1 ArF laser ablation

Glass has high absorption at 193nm wavelength and the threshold fluence required to cause material removal has been determined to be about 0.5-1 J/cm^2 based on prior studies. Therefore, in this research two laser fluence (5 J/cm^2 and 10 J/cm^2) with values greater than the threshold value was chosen for experimentation. Lower fluence excimer lasers (5J/cm^2) resulted in via diameter down to 19µm at 30µm pitch in 55µm thin borosilicate glass. Figure 66 shows the cross-section SEM image of TPVs fabricated using ArF based 193nm excimer lasers. Via profile was observed to be tapered, with measured entrance and exit diameter values of 19µm and 6µm respectively.

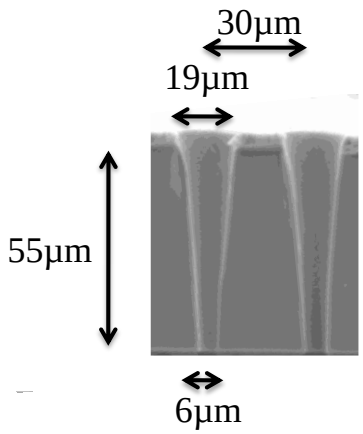
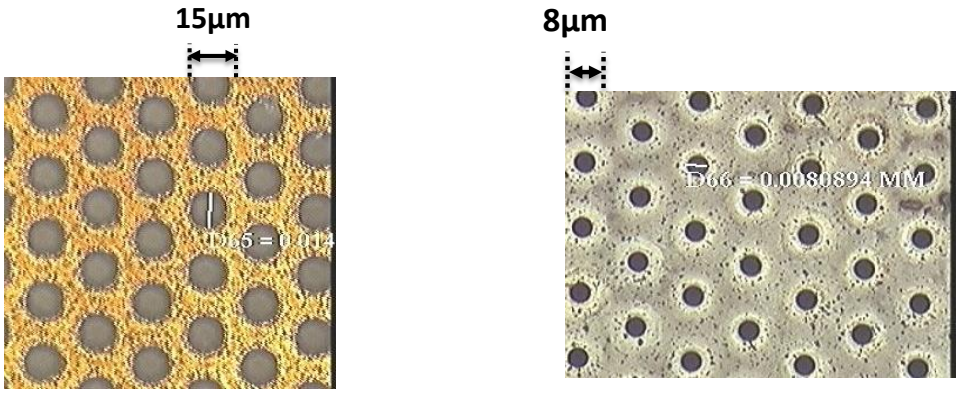


Figure 66: Cross-section SEM image of ArF laser ablation in 55µm thin BSG glass (courtesy: AGC Japan).

In addition to TPV formation using low-power excimer lasers, fundamental studies were carried out to understand via formation using high power excimer lasers. The sample used to study TPV formation comprised of a 30µm thin low-CTE glass laminated with a polymer layer (ZIF) having a thickness of 3µm. A high-power (10 J/cm^2) excimer laser operating in the frequency range of 10-50Hz was used, and the laser was irradiated over a sample size of 0.5mm x 0.5mm using a projection mask.

The optical image of the entrance and exit side of TPVs in thin glass substrate after laser ablation are shown in Figure 67a and b respectively. The measured dimensions of TPV entrance and exit diameters were 15µm and 8µm respectively and the via pitch was 27µm. The higher laser fluence (10 J/cm^2) of the excimer laser resulted in a more vertical TPV side-wall profile with reduced via-taper angle (84^o) compared to ablation at lower fluence [105]. This result is consistent with prior studies on via ablation using 193nm laser, which reported vertical TPV profiles at higher fluence, due to rapid accumulation of energy in the ablation zone and low dissipation of thermal energy though the glass substrate [42].



(a) **(b)**

Figure 67: Optical Image of ultra-small TPVs in 30µm thin glass: a) Entrance side with diameter of 15 µm, b) Exit side with diameter of 8 µm.

The ablation depth *(Δd)* per pulse can be computed using Beer's law in Equation 12.

$$\Delta d = \frac{1}{\alpha} \ln\left(\frac{Fi}{Ft}\right) \quad (12)$$

Where, 'α' is the absorption coefficient of glass, F_i is the incident laser fluence and F_t is the threshold fluence.

The absorption coefficient of glass (α) is a function of the material property and the wavelength of incident radiation [60]. The ablation depth per pulse *(Δd)* was computed as 271.5nm/pulse for incident laser fluence (F_i) of 10 J/cm^2, by assuming a value of 0.263 J/cm^2 for threshold fluence (F_t) and a value of 134000 cm^{-1} for absorption coefficient [42]. A linear relation between the etch depth (D) and the number of laser pulses (N) (Equation 13), suggests a total of 110 laser pulses for complete TPV ablation through a 30µm thin sample.

$$D = N.\Delta d \quad (13)$$

Experimental results verified that a total of 100-120 pulses were required to completely etch through 30µm thin glass. This result was observed to be consistent with the calculated value. The progression of via formation with increase in number of laser pulses is illustrated in Figure 68.

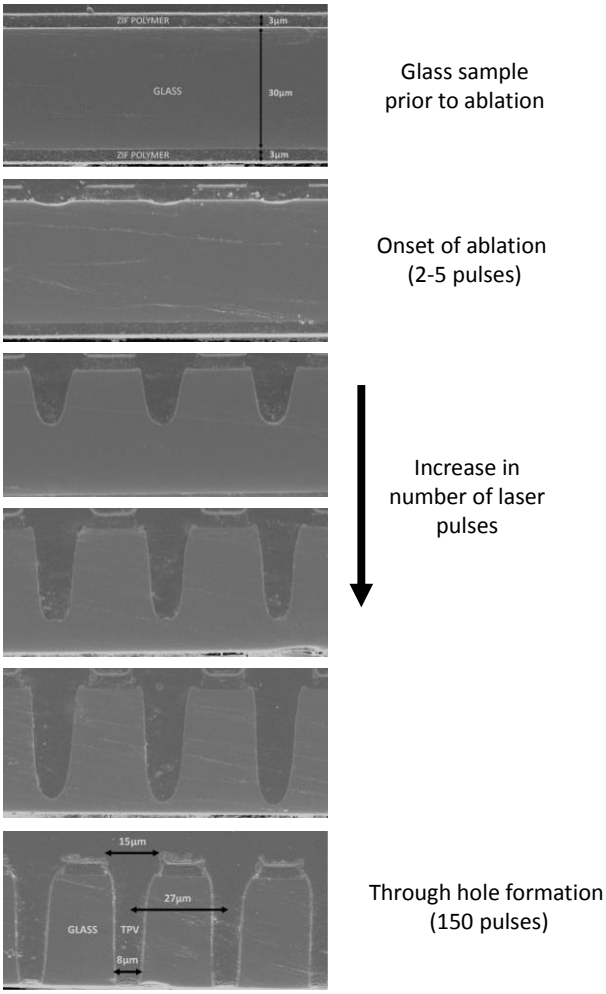


Figure 68: SEM image of TPV cross-section, showing ablation profile as a function of number of laser pulses using 193nm excimer laser ablation in 30µm thin glass.

Additional SEM observations were made on the TPV arrays formed in 30µm thin glass and the results obtained are illustrated in Figure 69. The TPV pitch was observed to be less than 30µm.

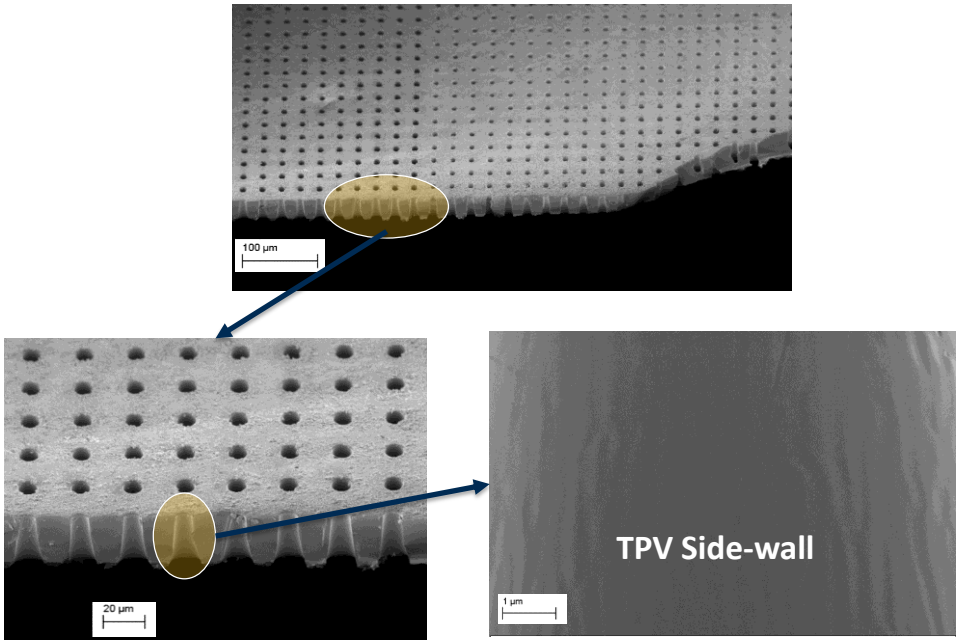


Figure 69: SEM images of array of TPVs formed in 30µm thin glass using 193nm excimer laser.

4.7.2 Effect of variation in pulse number on TPV dimensions

As described in the previous section, the amount of glass material that is removed from the bulk depends on the number of laser pulses incident on the sample. Further, it was observed that a minimum of 120 laser pulses would be required to completely etch through 30µm glass. This section studies the effect of variation in laser pulse number on the entrance and exit diameter of the TPVs. The material stack-up was identical to the one used in the previous section and comprised of 30µm thin glass laminated with a 3µm thin polymer film on both sides. The laser fluence was 10J/cm^2 and the number of laser pulses was varied from 120 to 150. A top view optical image of TPVs formed using different count of laser pulses is shown in Figure 70. The results indicate a constant entrance TPV diameter (15µm), while the exit diameter increased with increasing number of pulses.

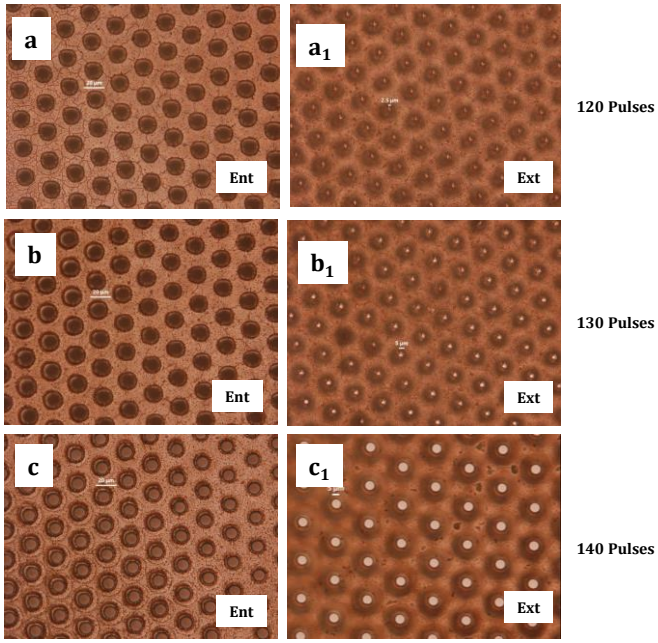


Figure 70: TPV entrance and exit diameter as a function of number of laser pulses at 10J/cm^2 fluence: a) 120 pulses b) 130 pulses and c) 140 pulses.

The variation of TPV taper angle as a function of the number of laser pulses is shown in Figure 71. The entrance diameter was observed to be invariant with number of laser pulses due to the small spot size and non-thermal nature of the ablation process that prevented the enlargement of via diameter on the entrance side (observed in the case of UV and CO_2 lasers). The exit diameter as mentioned earlier steadily increased with increase in number of laser pulses.

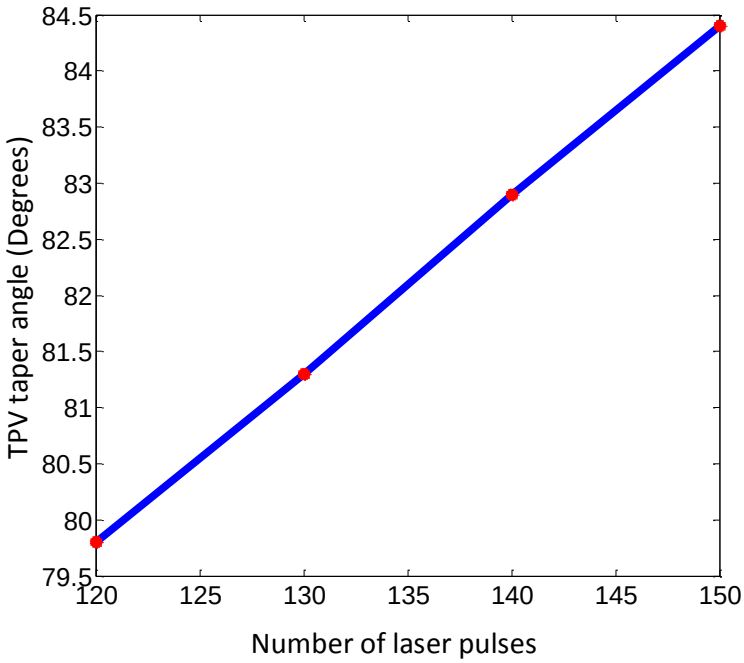


Figure 71: TPV taper angle as a function of number of laser pulses.

4.8 Through-put estimation of TPV formation in ultra-thin glass

Laser ablation using excimer lasers can be scaled to achieve higher through-put by using mask-projection technique.

In the mask-projection approach the laser beam is made to pass through a mask before being focused onto the glass sample. The mask can be patterned to achieve the desired via array and geometry. A schematic drawing of such a system is shown in Figure 72. As shown in the figure, a focused beam from the excimer laser is made incident onto a mask after passing through a set of deflecting mirrors. After the laser beam passes through the mask, a projection lens is used to focus the laser beam onto the sample glass sample to be machined. The feature size on the mask is de-magnified using a projection lens. The degree of de-magnification can be varied between 5X and 20X. A schematic diagram showing the demagnification concept is illustrated in Figure 73.

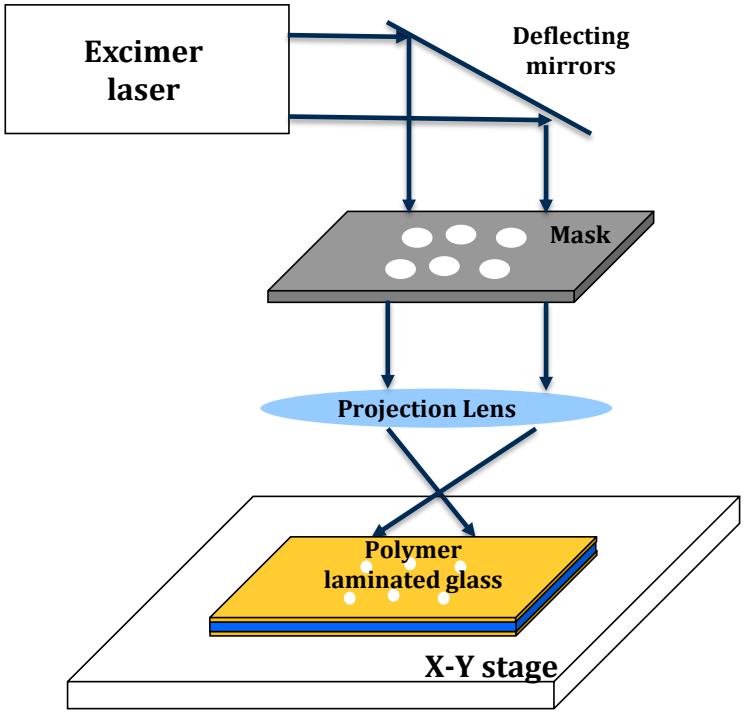


Figure 72: Excimer laser set-up: Mask projection technique.

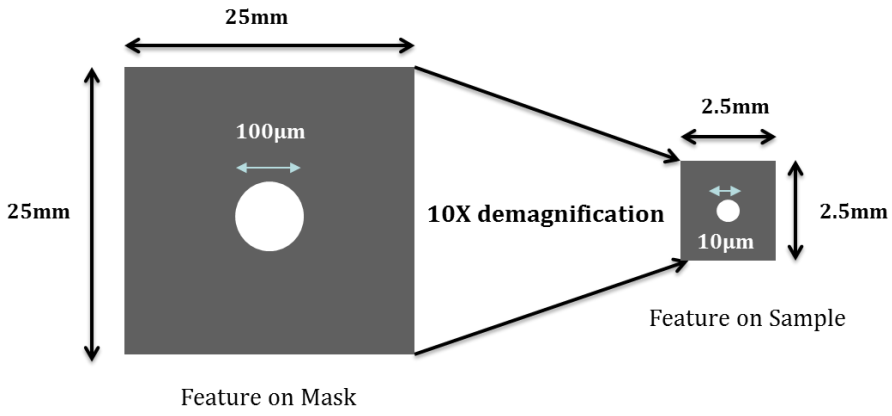


Figure 73: Principle of mask projection.

ArF based excimer laser operating at 193nm was used in mask projection mode; after passing through a metal mask. The metal mask is usually made of aluminum or brass and the ratio of the feature size on the mask and sample is 10:1. In other words, via opening of 300µm on the mask produces a 30µm spot size on the sample. The effect of two different excimer laser fluences (5 J/cm^2 and 10 J/cm^2) on via throughput was studied.

Using a mask projection technique an array of TPVs was drilled at 30µm pitch in 55µm thin glass. The irradiation area was 1mm x 1mm, and a total of 1089 vias was formed simultaneously. The measured entrance and exit diameters were 19µm and 6µm respectively. The total drill time was approximately 10 seconds, which corresponds to a throughput of greater than 100 vias per second. Figure 74 shows the top view optical image of an array of vias drilled simultaneously using the mask projection technique.

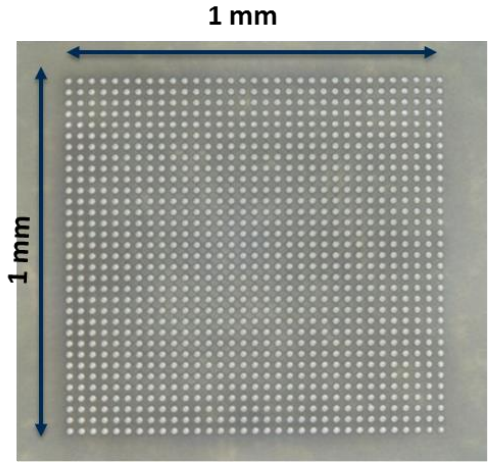


Figure 74: Top view optical image of an array of TPVs drilled in glass using the mask projection approach (Courtesy: AGC, Japan).

In order to study the effect of increasing laser fluence on via drilling, high power excimer laser (10 J/cm^2) ablation was explored on thin glass substrates (30µm). The number of laser pulses required to drill through the sample was 120 (N = 120) at 50Hz operation. Via diameters achieved were 15µm on the entrance side and 6µm on the exit side. Figure 75 shows the top view optical image of an array of 441 vias drilled simultaneously at 27µm pitch. The irradiation area on the sample was 0.6mm x 0.6mm, and the process time was less than 3 seconds (for 50Hz operation and 120 pulses).

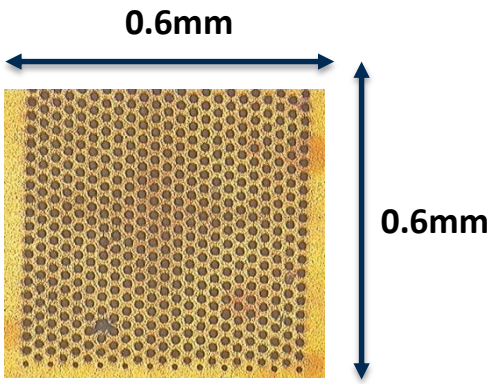


Figure 75: Array of 441 vias at 27µm pitch, drilled using high power excimer laser operating in mask projection.

A summary of the through-put capabilities explored using low and high power excimer lasers is shown in Figure 76.

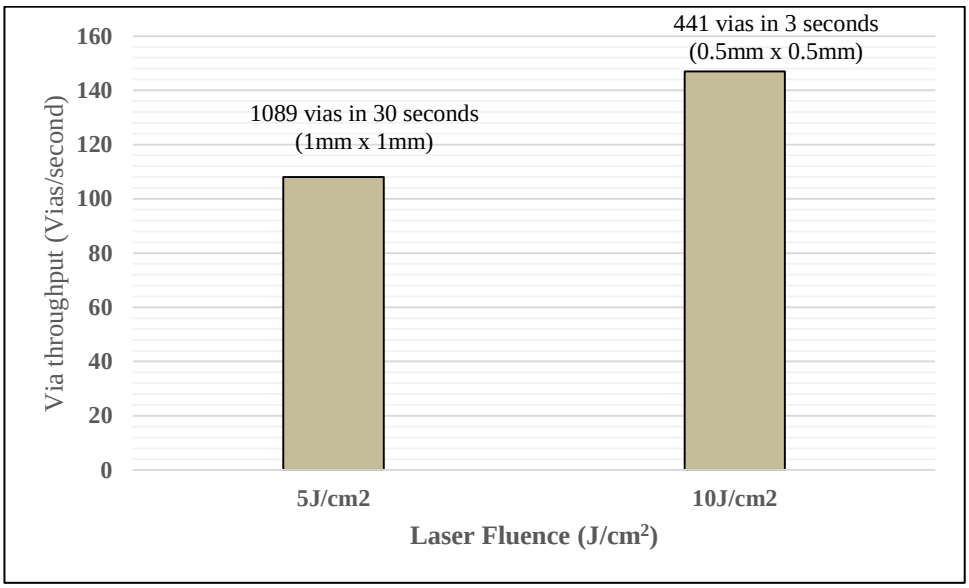


Figure 76: Measured TPV through-put at two different excimer laser fluences.

The study on TPV formation showed that excimer lasers can form small TPVs in thin glass substrates. However, from a cost a-nd manufacturing perspective it is necessary to evaluate the throughput of via formation. Higher throughput translates to shorter processing time which eventually leads to lower production cost. This section

studies and analyzes the feasibility of excimer lasers to operate in the mask projection mode to form several hundred vias simultaneously.

High-power excimer lasers (5-10J/cm^2) typically operate in the frequency range of 5Hz to 200Hz. Based on the result obtained as shown in Figure 75, an approximate prediction model is proposed for evaluating TPV throughput as a function of operating frequency. The models are proposed for three cases: 1) the number of laser pulses required to drill thought the sample remains constant (say N = 140), 2) the number of pulses required varies directly as the ratio of f_o to f, where f_o = 25Hz and f is the value at a given point within the frequency range, and 3) the throughput is independent of the laser operating frequency.

For the first two assumptions, the throughput value also depends on the laser irradiation area, and the geometry of via, in terms of TPV diameter and pitch.

Case1: In the case where a fixed number of laser pulses is required to etch through the glass of given thickness, the relation between via throughput and frequency is linear as shown in Figure 77. The slope of the graph shown in Figure 77 depends on the irradiation area and via geometry. The projected via throughput is approximately 2250 vias/second at 45Hz, for a 2.5mm x 2.5mm irradiation area and with a via pitch of 30μm.

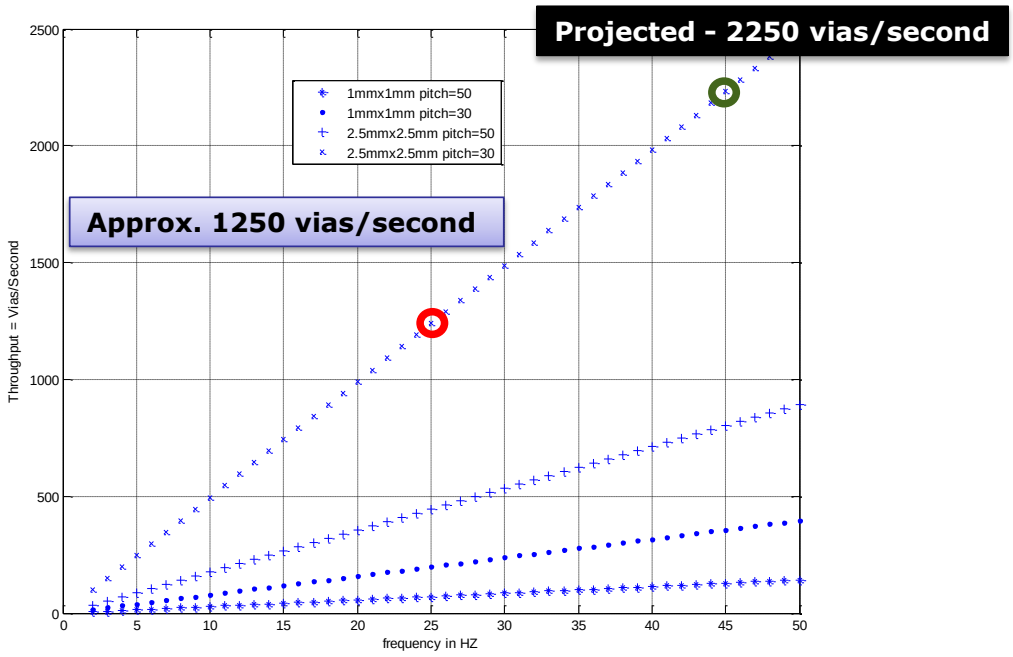


Figure 77: Graph of throughput v/s frequency; assuming the number of pulses required is constant.

Case2: The number of pulses required to drill thorough the sample is assumed to vary inversely with the frequency of incident radiation. This assumption is based on the logic that as the frequency of incident radiation is increased, the relaxation time between two consecutive laser pulses decreases. This could result in thermally assisted ablation of glass; requiring smaller number of laser pulses for ablation, at higher frequency. This model can be viewed as optimistic, with throughput predictions of approximately 4000 vias/second at 45Hz (Figure 79).

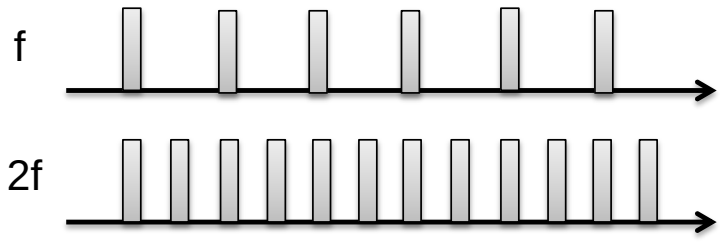


Figure 78: Incident laser pulse.

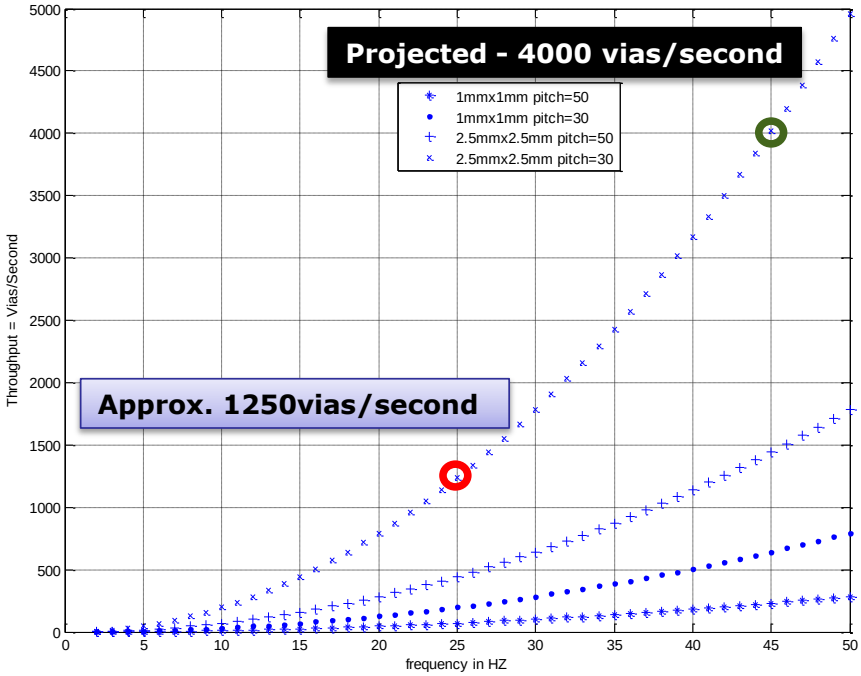


Figure 79: Via throughput v/s incident laser frequency, assuming inverse relation between number of pulses and incident frequency.

Case3: The third possibility is that the throughput is constant and does not vary with incident frequency.

Figure 80 shows the intersection of three graphs, based on the three cases discussed above. The actual throughput is predicted to lie in the shaded region bounded by two curves (invariant case and optimistic case).

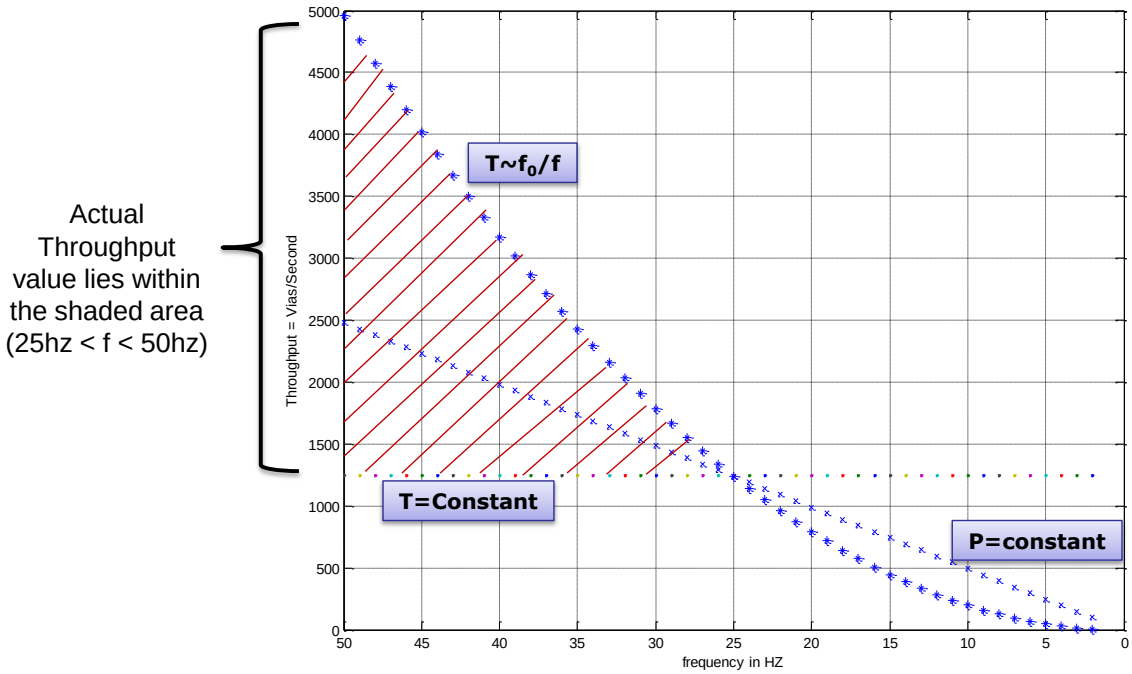


Figure 80: Graph showing via throughput prediction as a function of frequency.

Based on the experiments performed in 100µm and 30µm glass substrates, through-put measurements are presented. CO_2 laser ablation is a serial process with through-put values between 500-2000 holes per second depending on the desired quality of via hole. In case of excimer lasers an irradiation area of 2 mm x 2 mm is assumed. Also, it is assumed that the whole area is covered with TPVs. For excimer laser ablation in 100µm thin glass, it was observed that the total time required to drill through the glass sample was 12 seconds and 7 seconds using 248nm and 193nm lasers respectively. TPVs were formed at 50µm pitch which translates to a through-put value between 100-200 vias per second. However, when the glass thickness is reduced to 30µm it can be observed that the time required is significantly reduced. A total of 2.3 and 4 seconds were required to completely etch through 30µm glass using 193nm and 248nm lasers respectively. In addition, the study revealed that excimer laser ablation in thinner substrates can yield smaller TPV diameters (10µm) at 30µm pitch. Therefore the measured through-put value lies between 1000-2000 vias per second. The results described above are summarized in Figure 81.

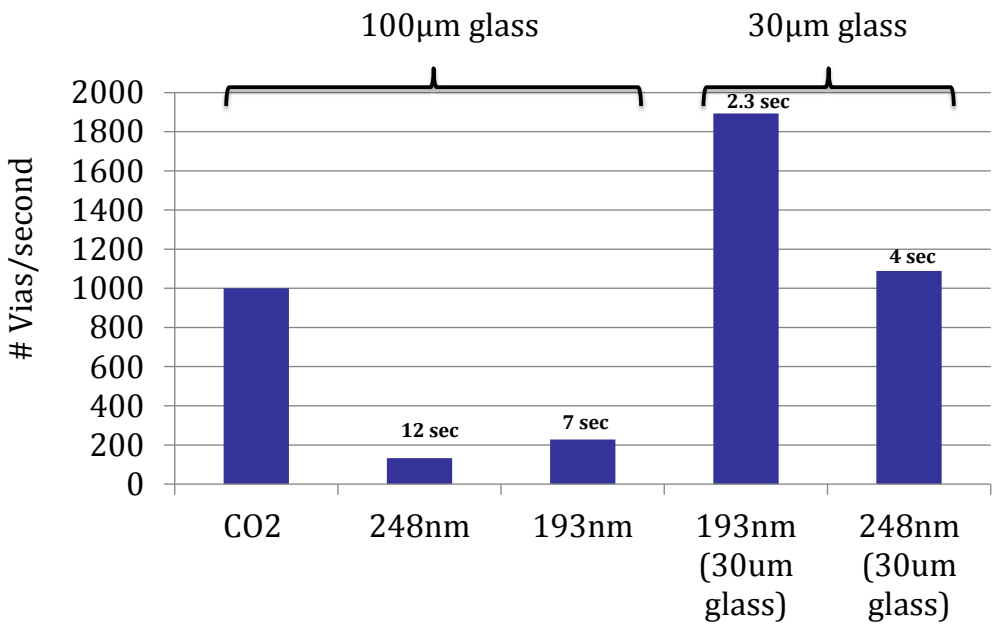


Figure 81: Measured through-put value of TPV formation using excimer and CO_2 lasers.

It has to be noted that actual interposer designs do not contain via array patterns throughout the sample. The time required to step and repeat over a larger panel size (> 150 mm x 150 mm) can be significantly higher compared to small area irradiation (10 mm x 10 mm). One method to improve the through-put is to increase the laser fluence which can lead to enlargement in projection area.

Additionally, there is a need to compare the through-put capabilities of excimer laser ablation to those obtained using DRIE etching. As explained in the first section of this chapter, DRIE is a slow process with etch rates of approximately 0.5-0.7µm/min. However when considering ultra-thin glass substrates (30µm) the DRIE approach presents an interesting process option to form small TPVs at higher throughput.

If one assumes an etch rate of 0.5µm/min for DRIE, the total time required to completely etch through 30µm thick glass is about 60 minutes. Thus, to form a single TPV using the DRIE approach would take approximately 60 minutes, compared to 1-3 seconds in the case of excimer lasers. However, with DRIE, TPVs can be formed

simultaneous using a patterned mask on the glass surface that could significantly reduce the processing time per TPV. A detailed study on DRIE etching on 30µm thin glass could be performed as part of future extension of this research.

4.9 Summary of TPV formation methods and process guidelines

This section summarizes the key finding from TPV formation study and proposes process guideline for via formation in 100-300µm thin glass substrates.

- Laser ablation is a promising method to form through vias in glass interposer. Since glass exhibits high absorption in the deep UV and infrared wavelengths, TPV formation was explored using excimer, UV and CO_2 laser ablation. Excimer lasers resulted in smallest via diameter (30µm) in 180µm thin borosilicate glass substrates.
- In order to achieve smaller TPV dimensions considering the side-wall taper from the laser ablation process, there is a need to migrate to thinner glass substrates. However, significant challenge exists in handling such thin glass during processing. To address this challenge, this research developed a novel polymer (RXP4M and ZIF) on glass approach prior to TPV formation.
- TPV formation was explored in polymer laminated glass substrates. In case of CO_2 laser ablation a 'copper-window' approach was studied and applied to reduce the thermal gradients during the ablation process. The copper window approach was not effective due to thin copper layer and high laser pulse energy. However, the damage to the polymer layer on the entrance side was greatly minimized by using a thin copper layer (without windows) prior to ablation.
- 193nm ArF laser ablation in polymer laminated glass resulted in 35µm diameter TPVs in 180µm thin glass.

Ultra-thin glass

- Excimer laser ablation in ultra-thin glass substrates (30μm) was studied using 193nm lasers. Initially the theory of excimer lasers was introduced, followed by experimental results and analysis.
- The use of high power excimer lasers (10 J/cm^2) yielded smaller TPVs having a diameter of 15μm on the entrance side. A parametric study was performed by varying the number of laser pulses and its effect on TPV taper angle was studied.
- The use of excimer lasers in the mask projection mode was studied and it was observed that several hundred vias can be simultaneous formed within 1 second. The last section of the chapter discussed about the through-put prediction and measurement of TPV formation using excimer lasers.

Chapter 5

TPV METALLIZATION

In the previous chapter the formation of small TPV holes (10-15µm) in ultra-thin glass substrates (30µm) using excimer laser ablation was described. This chapter discusses the fundamental approach to metallization of these small TPVs to achieve vertical interconnections with high electrical conductivity in 3D glass interposers. Copper was chosen as the metallization material because of its high electrical conductivity ($6x10^7$ S/m) and its ease of deposition using either the electroless or sputtered approaches. Moreover, the results from electrical modeling of TPVs presented in chapter 3 indicated that copper is the best material for achieving the lowest signal insertion loss and crosstalk. Metallization of TPVs with copper was performed using a semi-additive-plating approach consisting of two steps: a thin seed-layer using electroless deposition followed by electrolytic plating.

Direct metallization of glass poses significant challenges because glass is an oxide based material, it is chemically inert, and it has smooth surfaces. To form electrically conductive TPVs in glass, there are essentially two types of surfaces that need to be metallized: a) the planar glass surface on which to form the TPV pads and small-line width copper traces (redistribution layers) and b) the inside side-walls of TPV to form vertical interconnections.

Previous studies of bonding metals to glass (explained in chapter 2) involved sputtered seed-layers using either titanium (Ti) or chrome (Cr), which form excellent stable oxide interfaces and are commonly used to metallize directly on glass. Such physical and chemical vapor deposition techniques to deposit metals are already used to manufacture large panels. However, higher through-put methods such as plating processes are needed. The focus of this research is to explore electroless copper

deposition as a technique to achieve the necessary adhesion and to improve the overall throughput of metallization on glass interposers. In this research, two electro-chemical processes are explored: a) electroless copper for the seed layer and b) electrolytic copper plating to achieve the desired metallization thickness.

5.1 Theory of electroless copper deposition and electrolytic plating

In this research, a semi-additive-plating (SAP) approach using both electroless copper deposition and electrolytic copper plating was studied as the primary approach to achieve metallization of TPVs in glass interposers. A simplified process flow is shown in Figure 82 to illustrate the SAP process. As shown in this figure, the glass sample with TPVs was first subjected to electroless deposition to form a thin conductive layer of copper. Next, the sample was laminated with a dry-film photo-resist that was patterned using photo-lithography to expose the areas where additional copper is to be deposited through electrolytic plating. The photo-resist and copper seed layers were finally removed to realize metallized TPVs in glass interposers.

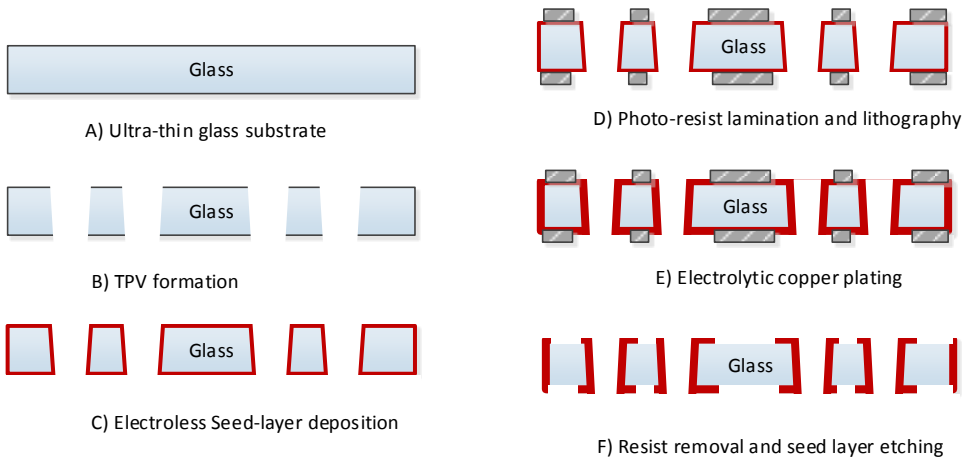


Figure 82: Semi-additive-plating process flow to achieve metallization of TPVs in glass

The electroless process does not require an external electric field for deposition. The chemical reactions that govern the electroless copper plating process are summarized below:

$$Pd^{+2} + Sn^{+2} \rightarrow Pd + Sn^{+4} \quad (14)$$

$$CuSO_4 + 2HCHO + 4NaOH \rightarrow \underline{\mathbf{Cu}} + 2HCO_2Na + H_2 + 2H_2O + Na_2SO_4 \quad (15)$$

Initially, the palladium ions in the activator solution are reduced to palladium atoms on the glass surface. This causes the appearance of the sample to change to a dark-grey color. Subsequently and in the presence of a reducing agent like formaldehyde (HCHO), the copper ions are deposited as copper atoms on the sample surface.

As Table 8 illustrates, in this study, a sequence of ten steps, which can be divided into three phases, was followed to achieve electroless deposition of copper. In the first phase (steps 1-3), the glass sample with TPVs was cleaned using a 'predip' solution to remove contaminants or residues from the sample surface. In the second phase (steps 4-7), the sample was then subjected to an activation step to form a thin and continuous layer of palladium (catalyst) throughout the sample surface, including the side-wall of the TPVs. In the third phase (steps 8-10), copper was deposited on the sample surface. A seed layer thickness between 0.7µm and 1µm was obtained after deposition for 30 minutes.

Table 8: Electroless copper deposition: Process sequence

Step number	Process	Function
1	Conditioner	Remove residues and soils from the surface and holes, conditions the glass and resin to ensure proper catalyst adsorption to these surfaces
2	Rinse	
3	Pre-dip	Protect copper contamination in the catalyst and provides common ion drag-in to the catalyst
4	Activator	Deposit palladium on the surface and wall of the hole. The

		palladium will then act as an activation site to initiate electroless copper
5	Rinse	
6	Rinse	
7	Reducer	Provides negative charges for reducing the copper ion to metallic copper
8	Electroless copper	Deposit a copper coating on the board surface and along the hole wall.
9	Rinse	
10	Acid Dip	Clean the copper surface

After the electroless deposition process was completed, the electrolytic copper plating process sequence was followed. In the electrolytic plating process, the set-up was comprised of a cathode, anode and an electrolyte in between. A schematic of the electrolytic plating apparatus is shown in Figure 83.

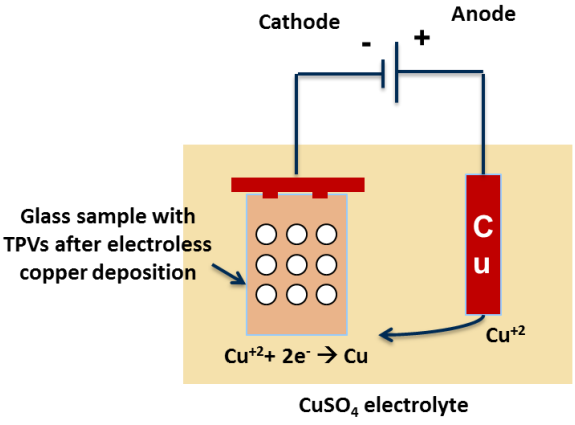


Figure 83: Schematic of the electrolytic plating set-up.

The cathode consisted of the substrate or interposer connected to the negative terminal of a DC source. The anode was a metal bar (Cu) connected to the positive terminal of the DC source. When an electrical field was applied, the copper cations

moved toward the cathode and were reduced to copper atoms on the substrate. The reduction reaction that occurs at the cathode is given below:

$$Cu^{2+}(aq) + 2e^{-} \rightarrow Cu^{o} \quad (16)$$

A specific process sequence was followed to electroplate copper. The sample was first cleaned prior to plating using an acid cleaner (Cupra pro S2) that helped remove contaminants and residues from the electroless surface. The Cupra pro S2 solution was heated to 40^{o}C, and the glass sample was immersed in this solution for five minutes. The sample was then thoroughly rinsed with DI water and subsequently immersed in an acid solution comprised of 10% volume of sulfuric acid. Next, the sample was mounted on a frame and subjected to electrolytic plating. The amount of copper deposited on the surface is a function of the current density and plating time. A simple equation was used to relate the plating time and current density to the thickness of plated copper.

$$\textbf{Plated copper thickness } (t_{Cu}) = \textbf{0.22x current density (ASD)x time} \quad (17)$$

The current density was determined by taking into account the total surface area of the frame and the surface area of exposed copper on the sample. A value of current density between 1.5 and 3 ampere per square decimeter (ASD) was used to achieve smooth Cu surfaces. An initial plating trial was performed to establish a guideline for the electrolytic plating process. The thickness of plated copper (over a 100 mm square sample) was measured as 10µm after 30 minutes while using a current density value of 2ASD.

5.2 Impact of surface roughness on TPV metallization

Initially, copper was deposited directly on the glass surfaces using the electroless process described in the previous section. However, the thin copper layer (< 1µm) easily delaminated from the glass surface during the rinse step that

immediately followed this deposition. On further inspection, it was found that the delamination occurred due to poor adhesion between copper and the smooth glass surface. This issue was addressed by roughening the glass surface prior to electroless deposition.

A photo-sensitive glass substrate having a thickness of 330µm was used for the initial trials. Through-vias were formed using a combination of UV exposure, high temperature bake and wet etching methods as explained in chapter 4. The measured diameter of TPVs was 100µm, and the spacing between vias was 75µm. To improve the adhesion between Cu and glass, the glass sample with vias was mechanically polished to increase its surface roughness. Surface profilometry was performed using laser confocal microscopy to study the topography of the roughened glass surface. The results obtained are illustrated in Figure 84 and Figure 85. The results indicated a surface roughness value (Ra) of few nano-meters in the case of smooth glass (Figure 85a), compared with a roughness value of few hundred nano-meters for mechanically roughened surfaces (Figure 85b).

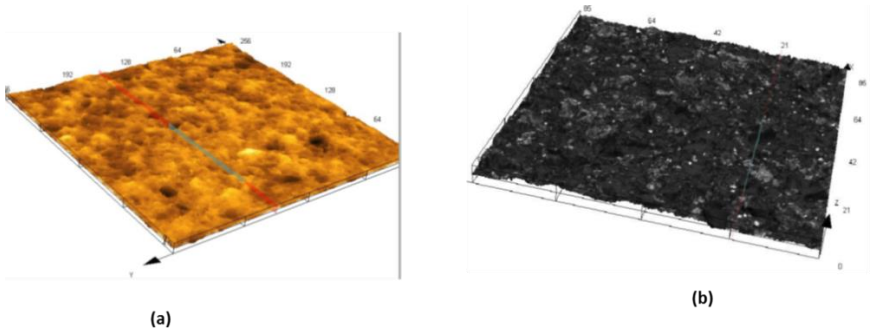


Figure 84: Laser confocal microscopy image of roughened glass surface: a) top surface, b) bottom surface.

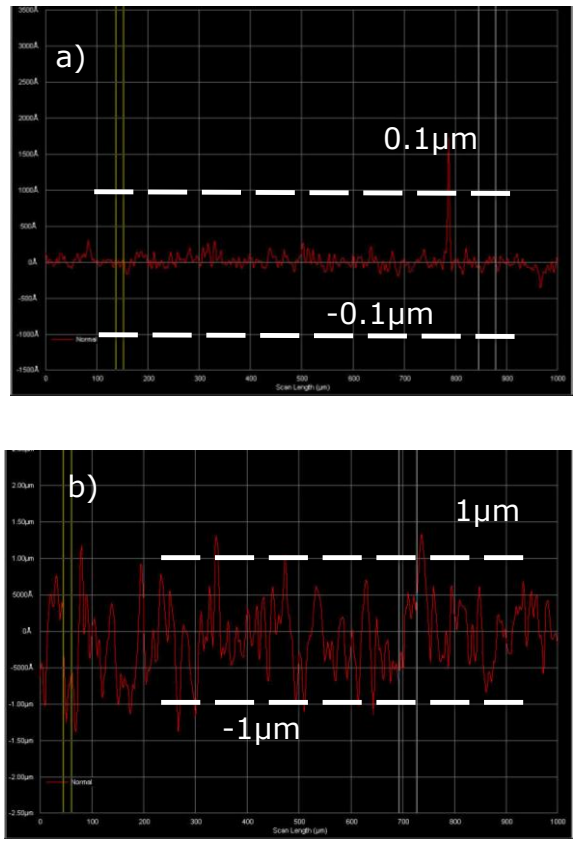
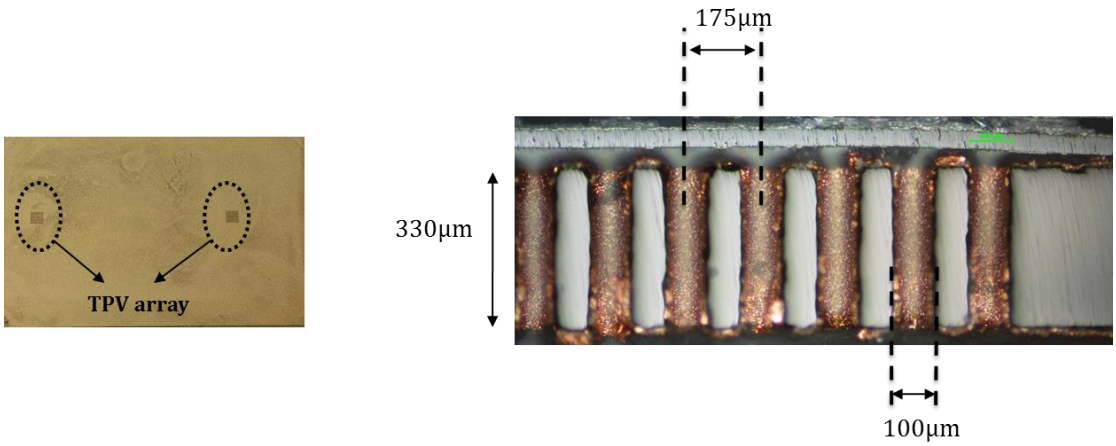


Figure 85: Surface roughness measurement data: a) smooth glass, b) roughened glass

The side walls of the TPVs, however, were not mechanically treated, and their roughness was completely due to the etch process (HF solution) used during via formation. Electroless copper deposition was carried out on the mechanically-roughened glass samples with TPVs. The adhesion between copper and roughened glass surface was significantly improved due to mechanical interlocking between the catalyst (Pd) and copper atoms. This improvement in adhesion strength was verified through the scotch tape test. An image of the glass sample after electroless copper deposition is shown in Figure 86. The observed improvement in adhesion was attributed to the increase in surface roughness and subsequent mechanical interlocking between the palladium catalyst and the glass surface. Further, the conformal deposition of copper in the TPV side-wall was also confirmed through cross-section examination, as shown in Figure 86b. A total copper thickness of 1µm was measured after electroless plating for 30 minutes.



(a) (b)

Figure 86: Electroless copper deposition on roughened bare glass sample with TPVs: a) glass surface showing TPV array, b) cross-section image of TPV array.

After electroless Cu deposition, the sample was subjected to electrolytic plating with Cu. The sample with TPVs was introduced as the cathode, and the anode was a metal bar made of copper. The electrolyte was a copper sulphate solution ($CuSO_4$). The value of the current used for the electrolytic process was 3A, which translated to a current density value of approximately 2.3ASD.

The measured copper thickness after electrolytic plating for 30 minutes was 5-7µm. A cross-section study on the TPV arrays confirmed uniform deposition of copper on the glass surface as well as on the side-walls of TPVs. An optical cross-section image of TPV arrays after electrolytic plating is shown in Figure 87.

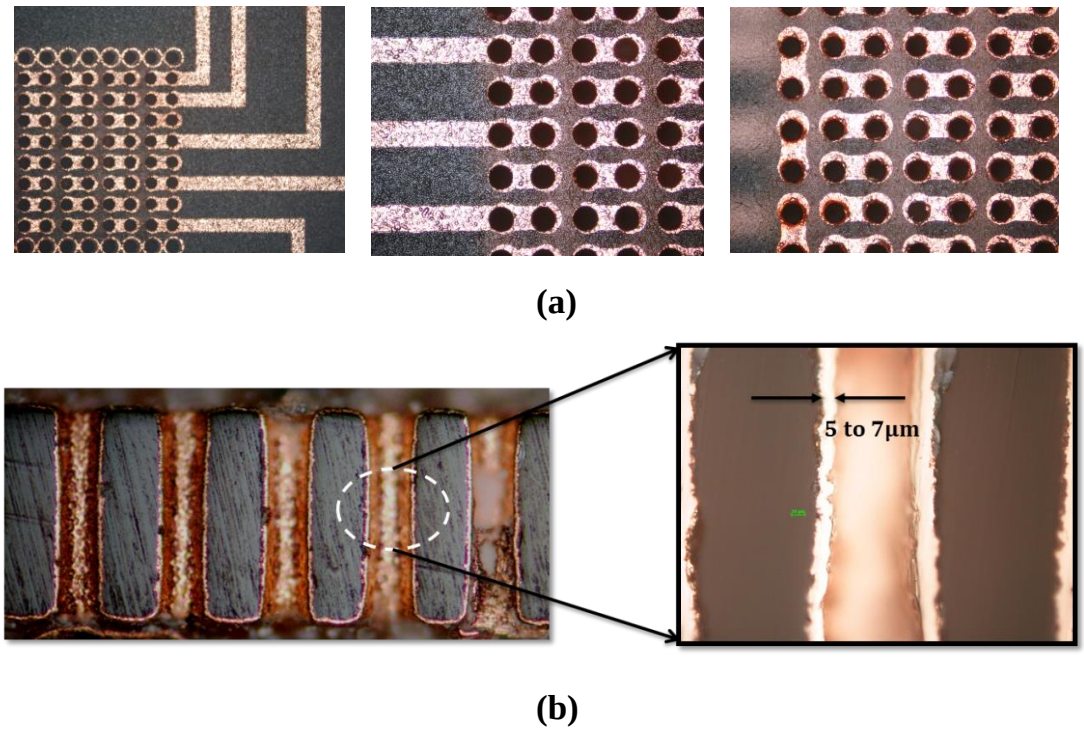


Figure 87: Metallization on Roughened Glass surfaces: a) RDL traces connecting TPVs on the surfaces and b) Cross-section of TPV array after electroplating.

In addition to the results presented in this research, Bamberg et al. from Atotech [106] in collaboration with researchers at Georgia Tech have studied copper metallization in roughened photo-sensitive glass substrates. Their study also reported good adhesion between the copper seed layer and TPV side-wall. In their study, the improvement in adhesion inside the TPV was attributed to the roughness induced during the via etch process. The images they obtained after cross-section examination are shown in Figure 88.

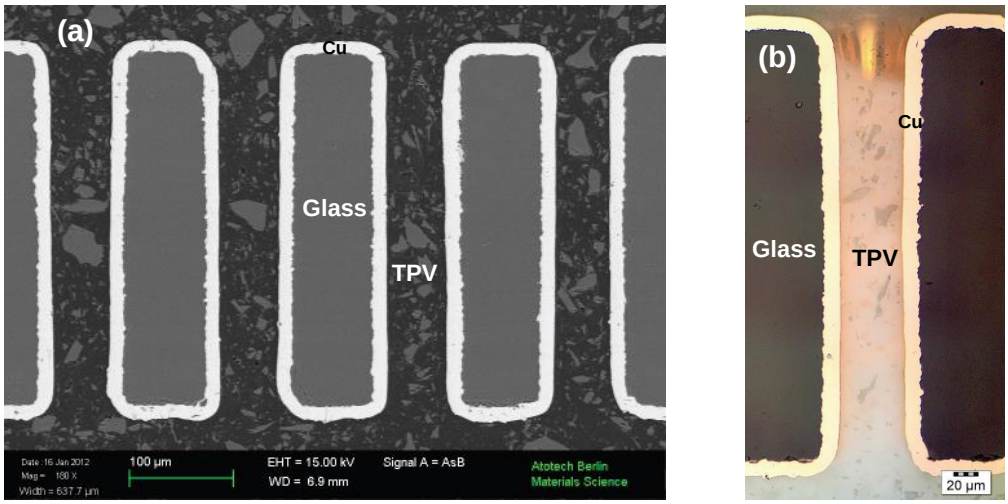


Figure 88: Cross-section image of TPV in photo structured glass after metallization: a) SEM image, b) optical image [106] [Courtesy: Simon Bamberg, ATOTECH Germany].

5.3 Metallization of TPVs in polymer laminated glass

5.3.1 Approach

Even though the adhesion strength can be improved by increasing the surface roughness, this adhesion strength must be good enough to withstand the CTE mismatch-related stress between glass and copper. Further, while roughening the glass surface, defects might be introduced that act as potential sites for crack initiation, growth and propagation. The CTE mismatch can lead to thermo-mechanical reliability failures at the glass-copper interface that can manifest as copper delamination or cracking in glass. As an alternative to glass roughening, prior studies have investigated surface modification techniques using self-assembled monolayers (SAM) of silane molecules [107, 108] to enhance the adhesion between metal and smooth glass surfaces. The mechanism involved the formation of Si-O bonds at the glass interface, wherein the alkoxy group of silane is attached to the glass surface while the functional group (amine) reacts with the catalyst such as palladium or tin. Although, good adhesion was observed for thin copper layers (150nm), an increase in metal thickness (> 1µm) resulted in delamination at the metal-catalyst interfaces.

However, for 3D interposer applications, the metallization thickness must be in the 3µm-10µm range to ensure a low resistance path for signal and power delivery through the interposer. Thus, silane treatment alone may not be conducive for achieving reliable metallization on glass interposers.

In the previous chapter on TPV formation, new thin-film polymers were laminated on glass surfaces for two main reasons: a) to improve the handling of thin glass and b) to minimize the defects created during the laser ablation processes. In the proposed approach, instead of the glass surface, the polymer surface is metallized for RDL and TPV pads, and the TPV side-wall undergoes changes in surface roughness from laser ablation, which results in improved adhesion between the plated copper and glass. A simple diagram is shown in Figure 89 that shows the conventional bare glass approach and the proposed polymer-on-glass approach investigated in this study.

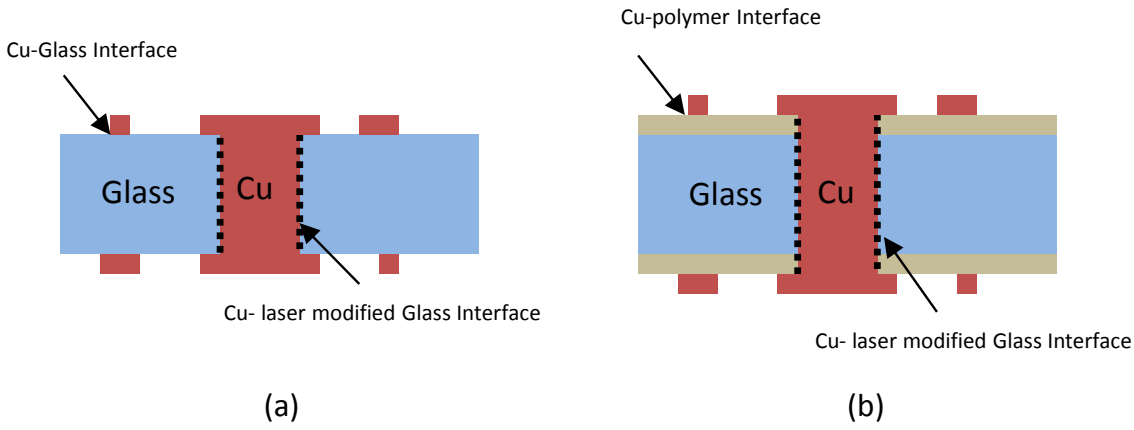


Figure 89: TPV in glass metallization: a) conventional approach, b) proposed approach.

The following section studies the metallization of TPVs in polymer-laminated glass substrates using the electroless and electrolytic processes.

5.3.2 Modified SAP process flow

In the case of polymer laminated glass substrates, a few additional steps were added to the SAP sequence. The modified process flow is illustrated in Figure 90. As indicated in this process flow, a thin polymer film (ZIF or RXP4M) was laminated on both sides of thin glass prior to TPV formation. An additional chemical desmear step was required to treat the polymer surface before electroless copper deposition.

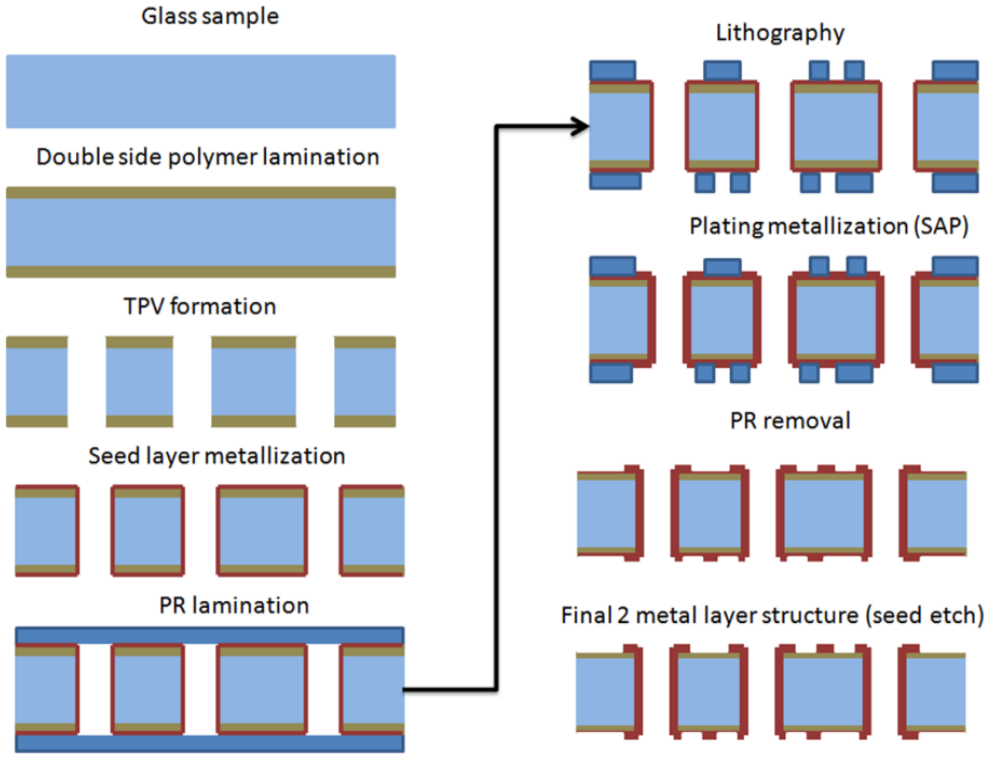


Figure 90: Modified process flow for SAP to metallize TPVs in polymer laminated glass.

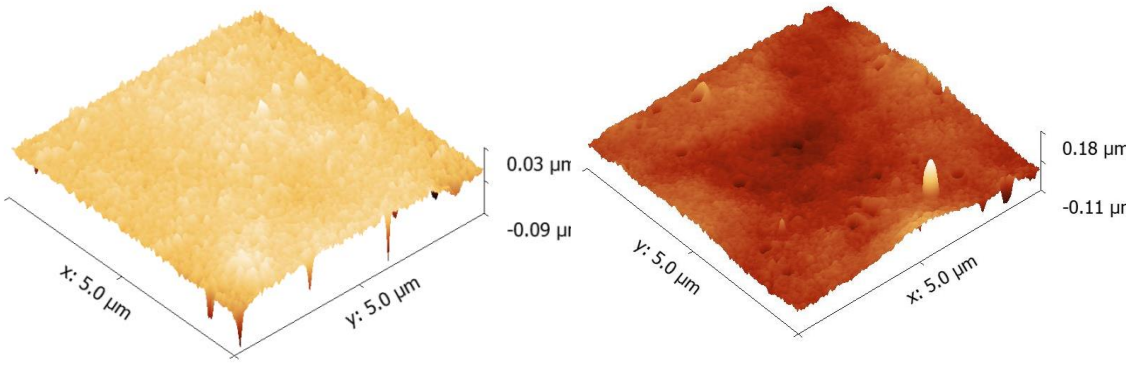
The desmear process roughens the polymer surface and enhances the adhesion between copper and polymer. In addition, the desmear step helps remove the debris that gets deposited on the polymer surface after laser ablation. In this study, the desmear process consisted of three general steps: a) swelling, b) desmear, and c) reduction. As explained in Table 9, the first step induced swelling of the resin (polymer) to facilitate efficient etching of polymer during the subsequent desmear step. Next, potassium permanganate ($KMnO_4$) was used to etch the polymer surface.

Finally, the reduction solution helped remove the permanganate residue from the polymer surfaces.

Table 9: Process sequence for chemical desmear of polymer dielectric on glass

Step number	Process	Function
1	Sweller	Swelling resin to ease the removal of smear by permanganate bath
2	Rinse	
3	Permanganate	Oxidize smear to be removed and roughen the surface of polymer
4	Rinse	
5	Reducer	Reduce remaining permanganate on a surface
6	Rinse	

The change in roughness of the polymer surface (ZIF) before and after the desmear process was measured using atomic force microscopy (AFM). The measurement was taken over a surface area of 25µm^2 (5µm x 5µm), and the results are presented in Figure 91.



Ra ~ 4.7nm

Ra ~ 14.9nm

(a) **(b)**

Figure 91: Polymer surface roughness measurements: a) before desmear and b) after desmear.

A significant increase in surface roughness (from 4.7nm to 14.9nm) of the polymer was observed as indicated in Figure 91.

After the desmear process, the samples with TPVs were subjected to electroless copper deposition and copper electroplating as explained in the previous section on metallization of TPVs in roughened photo-sensitive glass.

5.3.3 Metallization results

Using the modified SAP process explained in the previous section, the metallization of TPV formed by different laser ablation processes in polymer laminated glass was investigated. In the following section the metallization of TPVs formed using CO_2, UV, and excimer lasers are discussed.

The study on TPV formation in chapter 4 showed that smaller diameters TPVs can be obtained using CO_2 lasers that operate at high peak powers. High-peak power resulted in via diameters as small as 40μm in 100μm thick glass substrates. Such small TPV diameters were attributed to shorter laser pulse width, which resulted in significantly lower thermal damage. An optical cross-section image of TPVs after metallization is shown in Figure 92. The cross-section revealed the presence of heat-affected-zone (HAZ), which is highlighted by the dotted red circle in Figure 92. The HAZ was caused due to a combination of the high thermal energy released during the ablation process and the low thermal conductivity of the glass substrate (that limits the amount of heat dissipated through the bulk glass substrate).

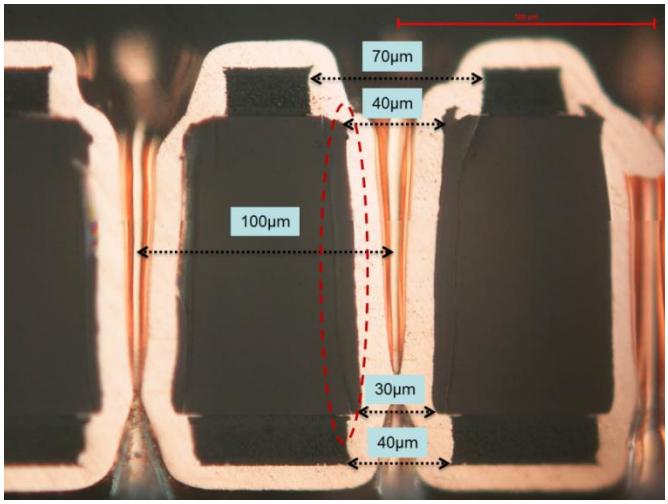


Figure 92: Cross-section image of metallized TPV formed using high peak power CO_2 laser ablation.

TPVs formed using UV laser ablation (355nm) in polymer laminated (RXP4M) glass were also metallized using the electroless and electroplating approach. The thickness of the plated copper was measured as 10µm. An SEM image of metallized TPVs is shown in Figure 93. As shown, the metallization resulted in a conformal deposition of copper inside TPVs with an aspect ratio of approximately 2:1.

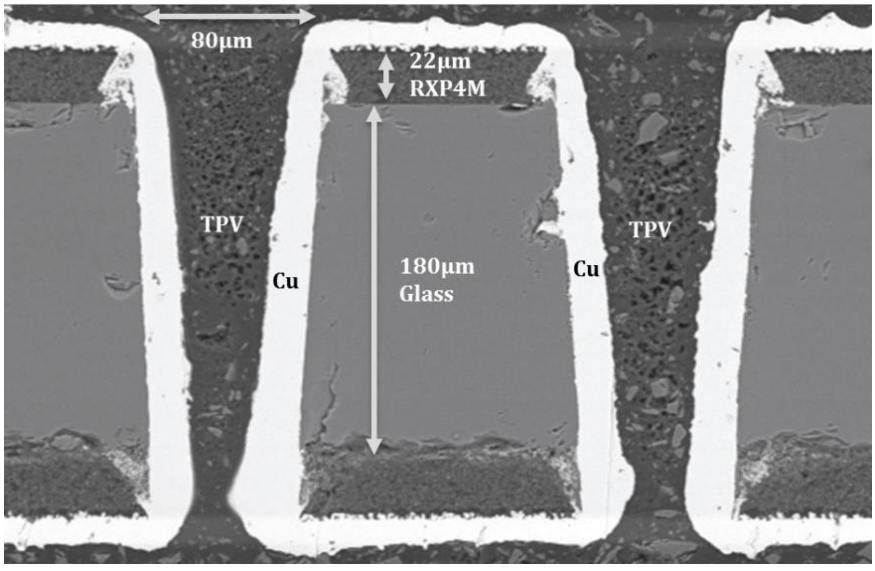


Figure 93: Cross-section SEM image of metallized TPV formed using UV laser ablation [Courtesy Atotech Berlin] [106].

In addition to UV ablated TPVs, the metallization of TPVs that were formed using excimer laser ablation was studied. The TPVs in polymer laminated glass (180µm in thickness) were formed using 193nm ArF laser with entrance and exit diameters of 60µm and 35µm respectively. The sample with TPVs was subjected to electroless copper deposition for 20 minutes, which resulted in a seed-layer thickness of 0.5µm. The sample was subsequently electroplated for 30 minutes to achieve a final copper thickness of 10µm. An SEM image of the TPV cross-section after metallization is shown in Figure 94.

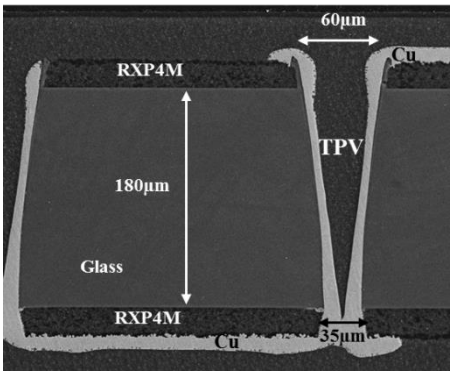


Figure 94: SEM image of metallized TPV with 60µm entrance diameter and 35µm exit diameter in 180µm thin glass.

Via formation using excimer lasers can be performed either from a single side of the glass substrate or from both sides. In the latter case, however, precise alignment accuracy of laser spots is required while ablating material from the top and bottom sides of the glass substrate. An optical cross-section image of metallized TPVs formed with: a) single side drilling and b) double side drilling are shown in Figure 95 and Figure 96 respectively. Double side drilling resulted in an 'X' profile as illustrated in Figure 96.

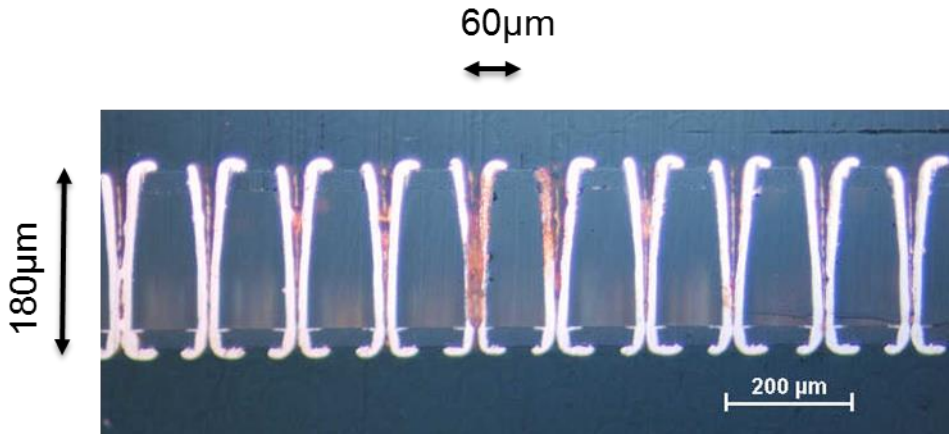


Figure 95: Cross-section image of metallized TPVs in glass formed using single-side laser ablation.

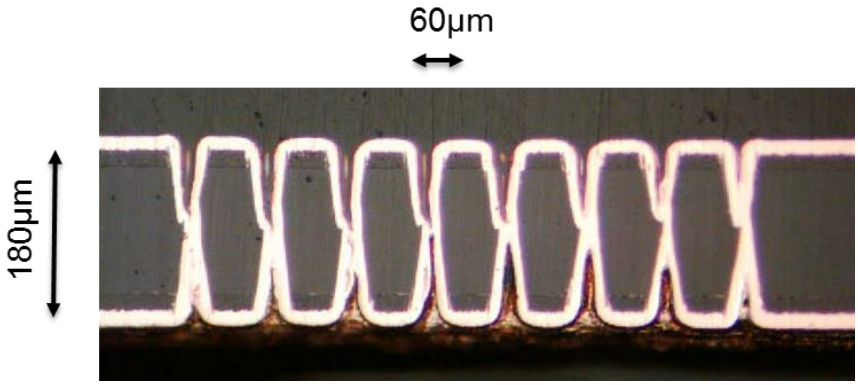


Figure 96: Cross-section image of metallized TPVs in glass formed using double-side laser ablation.

After studying metallization of TPVs in 100-180µm thin glass, the metallization study was extended to ultra-small TPVs in 30µm thin glass substrates. These thin samples were processed in the same chemical solutions used for 180µm or 100µm thin substrates. For the 30µm thin glass samples, the thickness of the ZIF polymer layers used was 3µm. Chemical desmear and electroless copper deposition were performed for a significantly shorter time for the 30µm thin glass sample with 3µm ZIF polymer compared to 100µm thick glass with 17-20µm ZIF polymer. Shorter desmear and electroless deposition time was used for two main reasons: a) to prevent complete etching or delamination of polymer from the glass surface and b) to

reduce the thin film stress in copper and thus decrease the probability of copper delamination from the polymer surface. Electroless copper deposition was performed for 5 minutes as opposed to the 20 minutes used for the standard process. A scanning electron microscope (SEM) image of an array of metallized TPVs in 30µm thin glass is shown in Figure 97.

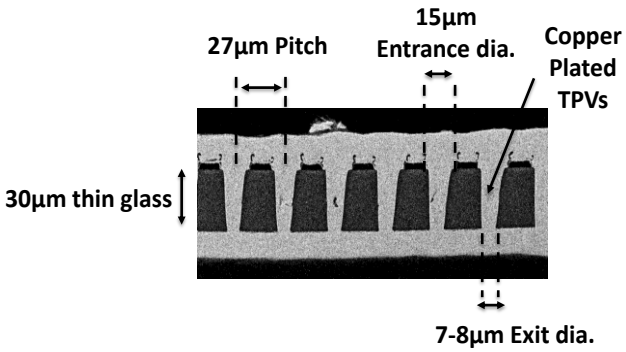


Figure 97: Cross-section SEM image of ultra-small metallized TPVs in 30µm ultra-thin glass.

5.4 TPV sidewall characterization

5.4.1 Cross-section and SEM observation

In studying the adhesion of copper to the TPV side-wall, the vias formed using excimer lasers were analyzed in greater detail after metallization. A detailed cross-section examination using SEM imaging was performed. A thin-layer of re-deposited material was observed around the TPV side wall, as shown in Figure 98. The volume of re-deposited material was observed to be greater on the entrance of TPV (Figure 98a) compared with the exit side (Figure 98c). This result can be explained by a mechanism that involves the ejection of molten material from the top side (entrance) of the TPV as a result of the high pressure created in the ablation zone.

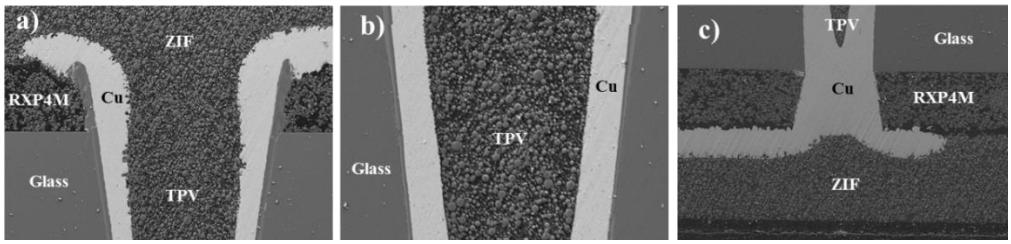


Figure 98: SEM cross-sections of metallized TPV in glass, showing re-deposited glass, a) TPV entrance, b) TPV middle, c) Exit side of via.

5.4.2 Mechanical property of re-deposited material along TPV sidewall

The surface morphology of re-deposited material was studied with regard to its mechanical property (modulus). The motivation for characterizing the re-deposited material was to have a better understanding of the mechanical behavior of TPV sidewall interface and the possible impact it may have on copper to glass adhesion and thermo-mechanical reliability.

Nano-indentation is commonly used for extracting the mechanical properties such as hardness of material surfaces, based on the load-displacement measurements as defined by:

$$H = \frac{Pmax}{A_r} \tag{18}$$

Where, H = Hardness

P_{max} = Maximum load applied

A_r = residual indentation area

An initial study using nano-indentation was performed on TPV cross-sections to study the mechanical properties of the re-deposited material. As shown in Figure 99, an array of 5x5 points was chosen for the indentation study. The spacing between adjacent indentation points was defined as 4μm and a maximum force of 2000μN was applied using a Berkovich tip with a known cross-sectional area.

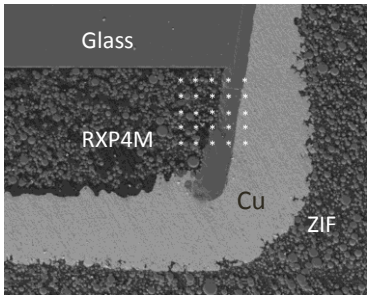


Figure 99: Cross-section of TPV, showing the nano-indented area array.

The measured load-displacement curves obtained from indentation measurements on the glass and polymer surfaces are shown in Figure 100 and Figure 101 respectively. As expected, the maximum displacement value for glass was observed to be much smaller (160 nm) compared with the polymer (475 nm). This result can be attributed to the lower modulus of polymer compared to glass.

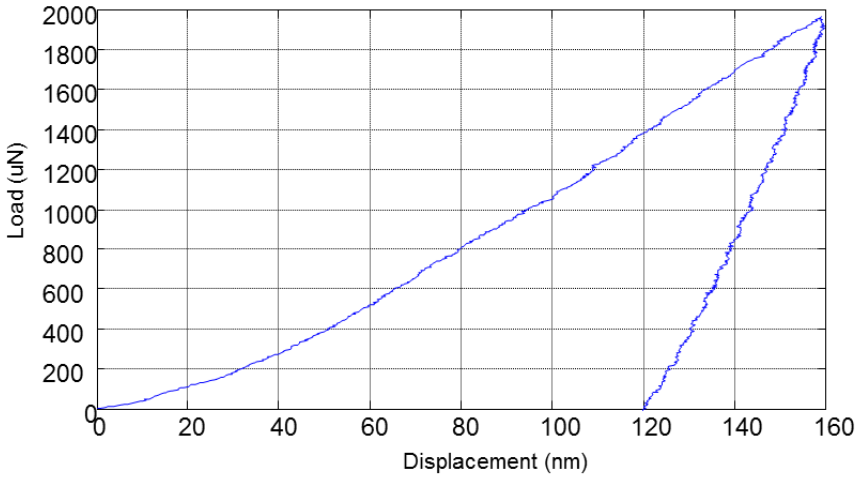


Figure 100: Measured load v/s displacement curve on glass.

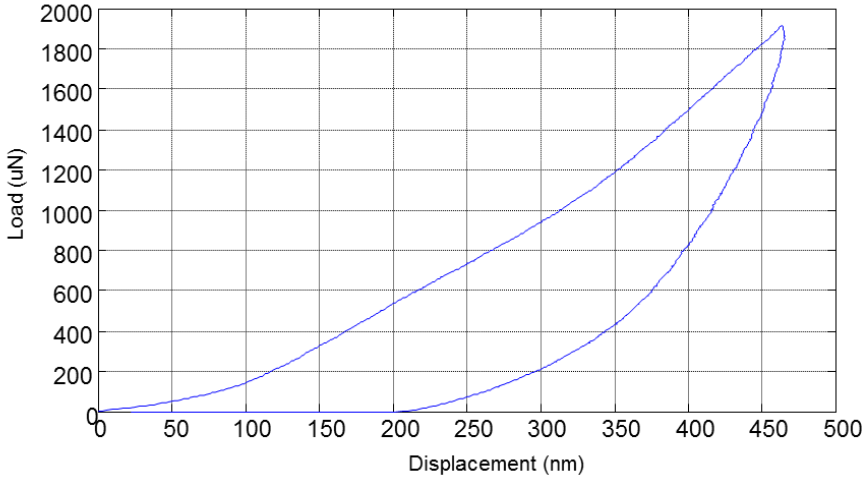


Figure 101: Measured load v/s displacement curve on polymer.

Young's modulus values were extracted from the load-displacement curves. The results obtained are summarized in Figure 102. The grouping of data points in Figure 102 indicates modulus values between 5-10 GPa, similar to the polymer surfaces, while a few points lie above 35 GPa, similar to bulk glass. A few anomalous points, for example, points 4, 14, and 19 were also observed. These Young's modulus values were slightly lower than the actual value of bulk glass, typically about 75-80Gpa. The softer nature of this deposited material implies that it may be a mixture of glass and polymer, which may have significant implications for glass-copper adhesion and reliability.

Additionally, a systematic nano-indentation study was carried out on the bulk glass and re-deposited material for varying indentation loads. The indentation tests were performed by Hysitron and the load-displacement data obtained are presented in Figure 103. From the load-displacement measurements, it can be clearly observed that the mechanical characteristics of the re-deposited material deviate from that of bulk-glass. This could lower the thermo-mechanical stress inside the TPVs and have a positive impact on TPV reliability. A more comprehensive study can be undertaken as

part of future extension of this research, to ascertain the chemical and mechanical property of the re-deposited layer.

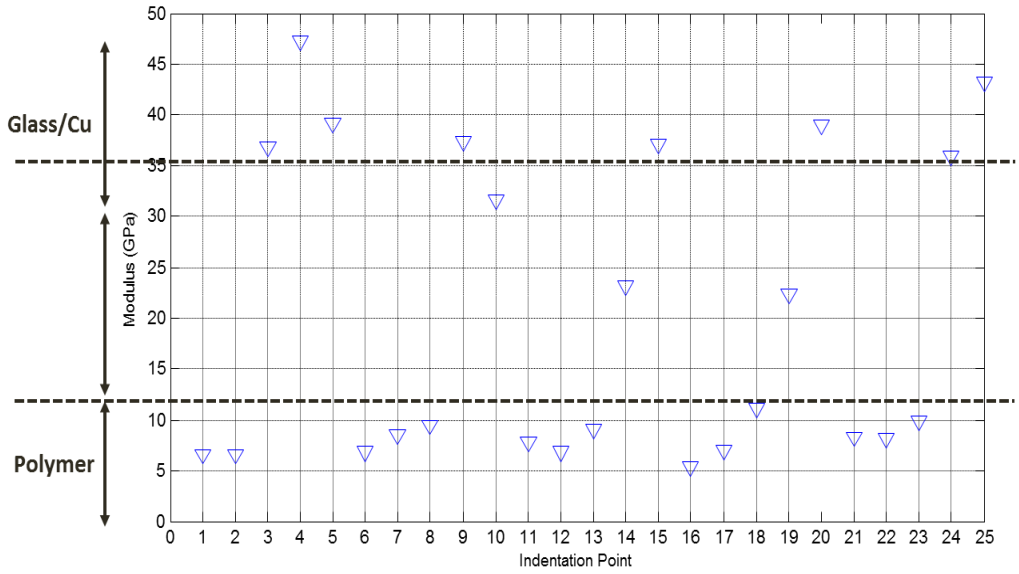


Figure 102: Map of modulus at each of the 25 indentation points.

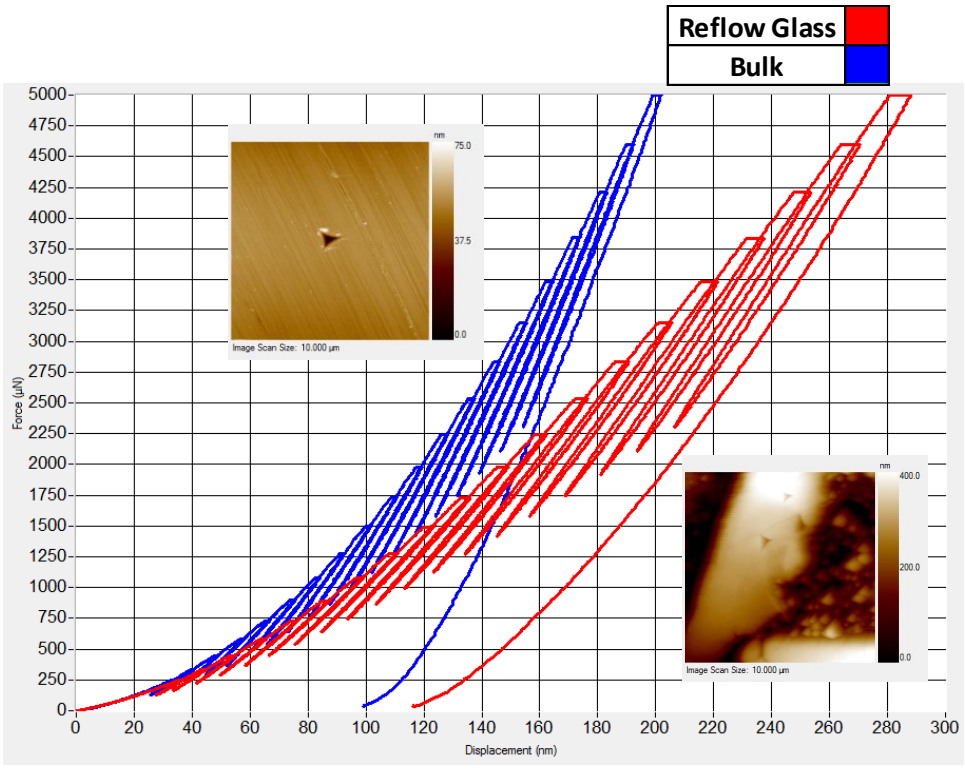


Figure 103: Load-displacement curves obtained from the indentation study on bare glass and on re-deposited material (Courtesy: Hysitron).

5.5 Thermo-mechanical reliability of TPVs

The thermo-mechanical reliability of TPVs in glass is critical for the overall performance of the glass package. As described in the previous chapter, TPVs are essentially made up of three materials: a) polymer (RXP4M or ZIF), which is laminated on the glass surface and present only on the glass surface (polymer is not present on the side-wall of TPVs); b) copper metallization inside the TPV; and c) glass as the material around TPV. Young's modulus and CTE values of glass, RXP4M polymer, and copper are provided in Table 10.

As indicated in Table 10, there is a CTE mismatch between copper, polymer, and glass that can cause stresses and result in catastrophic failures at one or more of the following interfaces: a) glass-copper, b) copper-polymer, or c) glass-polymer. At the glass-copper interface these stresses can result in glass cracking or copper delamination inside TPVs. Cracking of glass can result when the metallized TPVs are subjected to thermal cycles. The copper inside the vias expands and contracts more than the glass because of its higher CTE, resulting in glass cracking. Similarly, the stresses generated at the glass-polymer interfaces can cause delamination of polymer from the glass surface. Thus, a detailed study of the thermo-mechanical behavior of TPVs is important.

Table 10: Mechanical property of TPV materials

	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/^{o}C)
Glass	77	0.22	3.8
Polymer	1.83	0.3	67
Copper	121	0.3	17.3

An initial investigation of the thermo-mechanical reliability of TPVs in glass was undertaken in this study. A cross-section schematic of the TPV geometry

investigated is shown in Figure 104. The polymer used on the glass surface was RXP4M. The thickness of the glass substrates was 180µm, and the thickness of RXP4M polymer was 20µm. TPVs were formed using excimer laser ablation (193nm ArF laser). The choice of excimer laser in this study is due to the fact that these lasers yielded the smallest TPVs in glass with dimensions similar to TSVs in 3D ICs (based on the study in chapter 4). The TPVs studied in this section have an entrance diameter of 60µm and exit diameter between 30-35µm. Via pitch was defined to be 120µm.

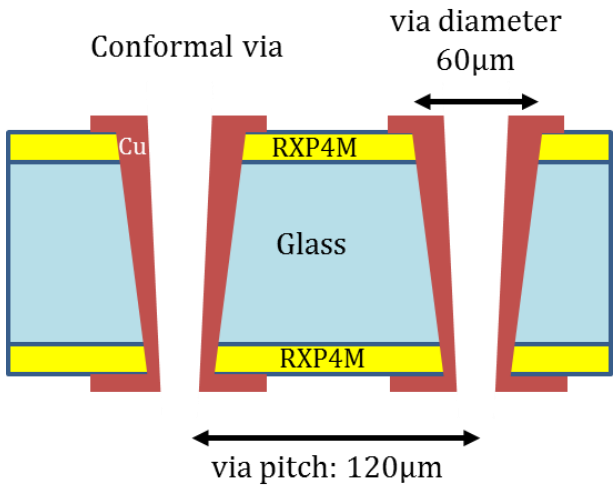


Figure 104: Cross-section schematic of metallized TPVs for reliability study.

5.5.1 Fabrication of TPV daisy chains

Low CTE glass (3.8 ppm) substrates (ENA1 from Asahi Glass) having a thickness of 180µm were used for fabrication. The glass was laminated with 20µm thick RXP4M polymer. An array of TPVs (8 x 6) was formed through this stack-up using 193nm excimer laser (in the mask projection mode). The use of mask projection resulted in simultaneous ablation of 48 vias within the array with measured via diameter and pitch of 60µm and 120µm respectively. The vias were subsequently metallized with copper and connected in a daisy chain pattern for measuring the resistance of the TPVs. The target metal thickness of copper was defined as 10µm.

Probe pads were designed at the end of each row within the array to measure the daisy chain resistance. A snapshot of the sample after fabrication is shown in Figure 105. A cross-section image of metallized TPVs connected in a daisy chain pattern is shown in Figure 106.

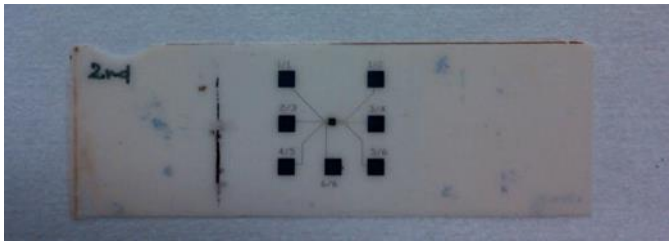


Figure 105: Glass sample with daisy chain pattern after fabrication.

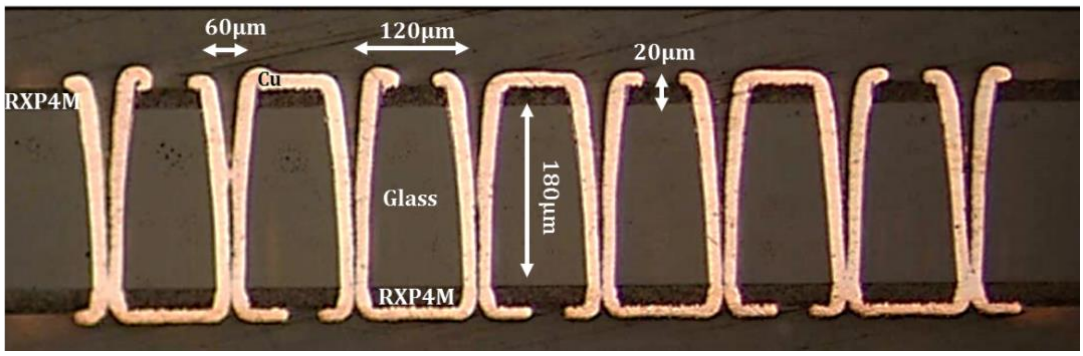


Figure 106: Cross-section image of TPV daisy chain after fabrication [23].

5.5.2 Test conditions and results

Metallized TPVs were subjected to thermal-cycle tests in accordance to JDEC (JEDEC JESD22-A104 condition B) standards, and daisy chain resistances were recorded over 1500 thermal cycles. The TPV daisy chains were first subjected to preconditioning that consisted of 3 steps: a) baking at 125^{o}C for 24 hrs, b) MSL3 for 40 hrs at 60^{o}C and 60% relative humidity, and c) 3X reflow at a maximum temperature of 260^{o}C. After preconditioning, the samples were placed in a thermal cycle chamber, and subjected alternately to low (-55^{o}C) and high (125^{o}C) temperatures with a dwell time of 30 minutes at each extreme temperature set point.

This varying temperature profile used for the TCT test is graphically shown in Figure 107.

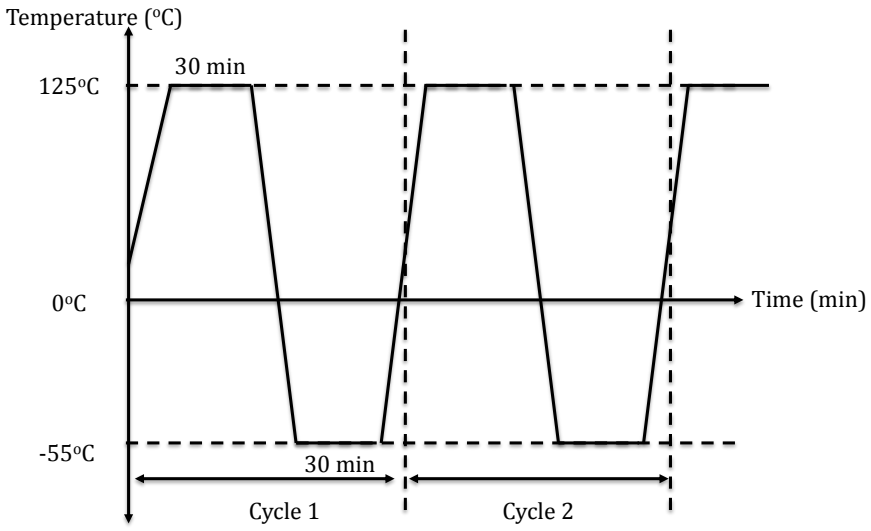


Figure 107: Temperature profile used for TCT testing.

The daisy chain resistance was monitored after every few hundred thermal cycles using a multimeter. The measured values represented a summation of eight TPV resistances within the chain, including the resistance of the copper traces connecting adjacent vias. A plot of these daisy chain resistance values over 1500 cycles is shown in Figure 108. As the data indicates, the resistance values (1-4 Ohms) of TPVs remained stable through 1500 thermal cycles. Minor variations in resistance values between the different daisy chains can be attributed to variations in plated copper thickness inside the TPVs.

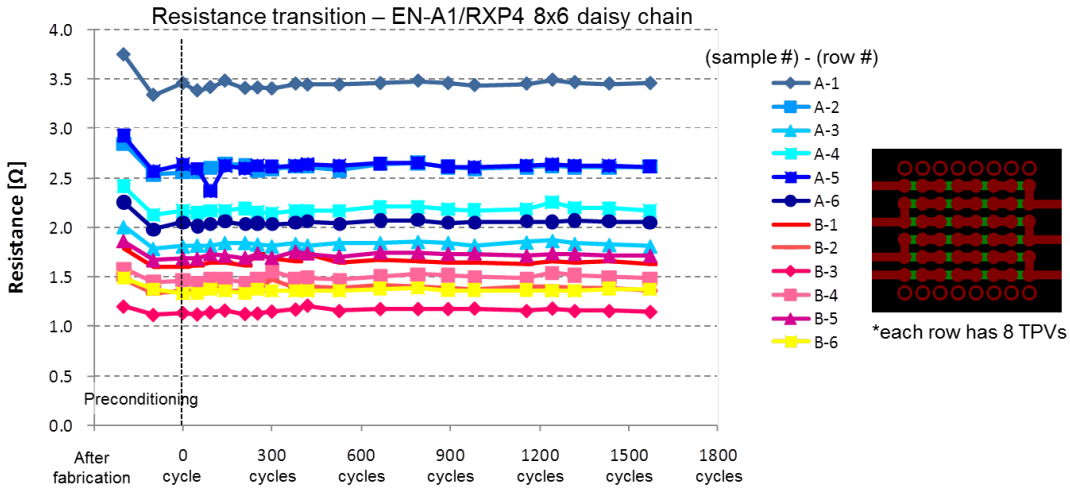


Figure 108: Daisy chain resistance after 1500 TCT cycles.

5.5.3 Post reliability analysis

After thermal cycle testing, the samples were subjected to failure analysis to detect cracks in glass or copper as well as to check for delamination at the interfaces. A typical 3D X-ray image after 1572 cycles is shown in Figure 109. These studies did not reveal any cracks or delamination of copper within the TPVs.

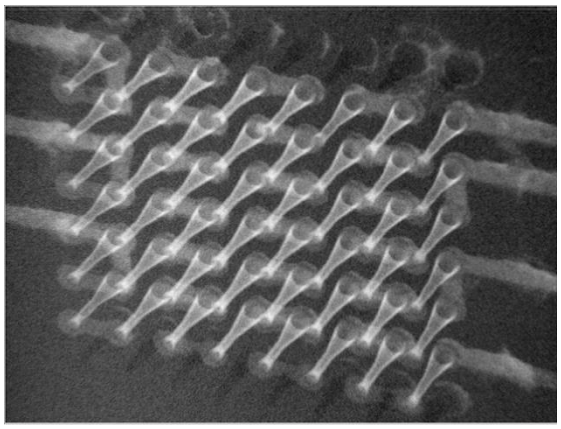


Figure 109: 3D X-ray image of TPV array after 1572 cycles.

To further confirm the results of the failure analysis, cross-section examinations were performed on the TPV daisy chains. The optical image obtained after polishing is shown in Figure 110. This cross-section image confirmed the results

from 3D X-ray imaging. In addition, no macro-cracking in glass was observed after 1500 thermal cycles.

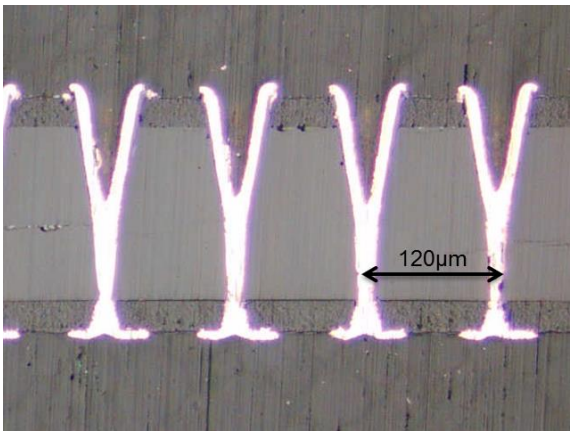


Figure 110: Cross-section of TPV array after 1500 TCT cycles.

The stable resistance data and absence of glass cracking after 1500 thermal cycles shows good adhesion between glass and copper and low stress due to mismatch.

5.6 Summary

a. Metallization study

- The metallization of TPVs in glass was studied as reported in this chapter. A semi-additive plating approach consisting of electroless copper deposition and electrolytic plating was used in this study. The theory behind each of these electro-plating technologies was introduced followed by experimental results.
- The use of thin-film polymer layers on glass surfaces had many beneficial effects including improved glass handling, defect-free TPV hole formation, lower stress at the interfaces and improved thermo-mechanical reliability through reduction of stresses at the corners of the TPVs.
- Metallization of TPVs in polymer-laminated thin glass was studied. The polymer was subjected to a desmear process using permanganate solution to enhance the adhesion between the electroless seed layer and polymer. Complete coverage of

copper seed layer on the surface as well as on the side-wall of the TPVs was achieved after the electroless process.

- TPVs with electroless copper were subsequently metallized using electrolytic copper and complete TPV metallization was achieved even in small TPVs (15µm diameter) (formed using 193nm excimer laser ablation) in 30µm thin glass substrates.
- A detailed cross-section examination of TPVs was conducted after copper metallization to study the various interfaces. The side-wall of TPVs (formed using excimer laser) showed a thin layer of re-deposited material. The mechanical property of this layer was analyzed using nano-indentation tests. These initial tests revealed that the re-deposited material had intermediate properties between polymer and glass which could impact copper adhesion to glass. Further study is necessary to ascertain the property of this interface and its impact on reliability.

b. Reliability study

- Preliminary reliability tests were performed on TPV daisy chains in polymer laminated glass substrates to understand their thermo-mechanical behavior.
- TPV daisy chains were subjected to thermal cycling tests (TCT) between -55^{o}C to 125^{o}C and showed stable daisy values through 1500 thermal cycles.
- Cross-section and X-ray examination after TCT did not reveal any cracks on the bulk glass or copper delamination from the TPV side-wall.
- A more comprehensive reliability study with detailed failure analysis is being undertaken by another Ph.D. student.

Chapter 6

ELECTRICAL CHARACTERIZATION

In chapters 4 and 5, the formation and metallization of ultra-small TPVs in glass were discussed. The TPV formation and metallization research was organized into two sections, with the first part focusing on various glass thicknesses and via formation methods, and the second part focused on the thesis targets of ultra-thin glass and ultra-fine pitch TPVs. This chapter presents the integration of the TPV processes with re-distribution layer (RDL) fabrication to form glass interposers ready for chip and board-level assembly, and is organized into two parts similar to the previous chapters. In the first part, the process integration methodology for two and four metal layer glass interposers (180µm and 100µm thick glass) with TPVs (formed using excimer laser) and their application in RF filters is discussed. In the second part, the electrical characterization results of small TPVs in 30µm thin glass substrates are presented.

6.1 Multi-layer glass interposers – materials and processes

In this study, thin glass substrates having a thickness of 100-180µm were explored, and novel-polymer materials that were introduced in chapter 4 was used as the build-up material.

The process flow schematic for two-metal layer glass interposer fabrication is same as explained in chapter 5 for TPV metallization illustrated in Figure 90. The thin glass (180µm) samples (150mm x 150mm) were cleaned using acetone and isopropyl alcohol (IPA) followed by rinsing with deionized water. The samples were baked for 30 minutes in air at 120°C to remove moisture. Subsequently, the glass surface was treated with silane coupling agents (3-Aminopropyltrimethoxy silane) to promote polymer to glass adhesion through the formation of -Si-O-Si- bonds at the interface.

The nature of chemical bonds and modification of glass surface chemistry after silane treatment is schematically shown in Figure 111. Si-O bonds are formed on the glass surface and the functional group (---NH_2) reacts with the polymer-chain molecules.

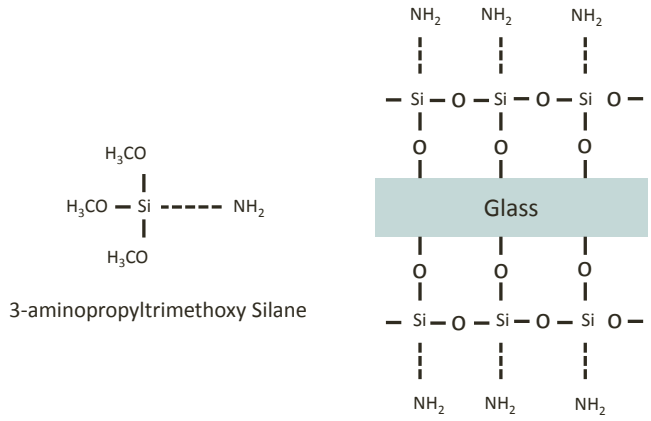


Figure 111: Silanization of glass for improved polymer to glass adhesion.

The absence of silane coupling between polymer and glass could lead to adhesion failures resulting in polymer delamination during subsequent chemical processing steps. To study the effect of silane treatment on polymer adhesion, two glass samples (one with silane treatment and the other without) were laminated with ZIF polymer. A snapshot of the polymer laminated glass samples after chemical desmear and electroless copper deposition is shown in Figure 112.

(a) (b)

Figure 112: Effect of silane treatment on polymer-glass adhesion: a) untreated glass, showing Polymer delamination from glass during chemical desmear process, b) Silane treated glass that shows improved adhesion of polymer to glass.

It was observed that in case of glass without silane treatment, polymer delamination occurred during subsequent chemical desmear and electroless copper

seed layer deposition. However, in case of silane treated glass surface, improved polymer to glass adhesion was observed which resulted in successful deposition of copper seed layer as shown in Figure 112b. In addition, the silane treated glass sample successfully passed the scotch tape test.

The polymer on the glass surface was either ZEONIF or RXP4M. In the case of RXP4M, a hot-press-lamination tool was used for lamination onto the glass surface. For a 150mm square glass sample, a pressure of 140 psi was applied for 90 minutes, at a temperature of 232^{o}C. The temperature profile used for RXP4M lamination is shown in Figure 113.

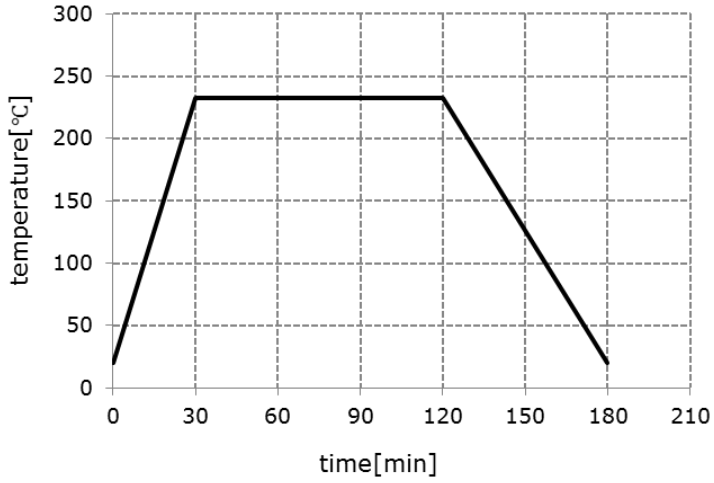


Figure 113: Temperature profile for RXP4M lamination on glass.

A steady temperature ramp was applied to the glass sample during the heat and cool-down cycles to minimize the stress on glass due to temperature gradients. The lamination of RXP4M required a slightly higher temperature (232^{o}C) and pressure compared to ZIF lamination (180^{o}C). The process was optimized to achieve a defect free glass surface which was devoid of cracks, as shown in Figure 114.

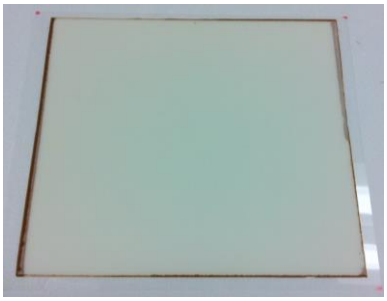


Figure 114: 150mm x 150mm glass sample after double side RXP4M polymer lamination on 180µm thin glass.

After polymer lamination, the next step in the fabrication process was the formation of small TPVs in the glass. Based on the study on via formation in thin glass, it was observed that excimer lasers are most preferred for the formation of small via holes. ArF based excimer lasers (193nm) were used to form TPVs, using the mask projection approach. Different TPV mask patterns were used to form the vias in polymer-laminated glass. The measured TPV entrance and exit diameters were 60µm and 35µm respectively. A snapshot of the test-vehicle after TPV formation using two different mask patterns is shown in Figure 115. Mask 1 has an array of four vias at 300µm pitch, while mask 2 has an array of 64 vias at 120µm pitch. Thus, based on the design a combination of mask 1 and mask 2 was used to form vias over the 150 mm square glass panel, using a step and repeat approach. The field size of a single shot was 1mm x 1mm, based on the output power of the laser ($4J/cm^2$) to ensure sufficient laser fluence for ablation.

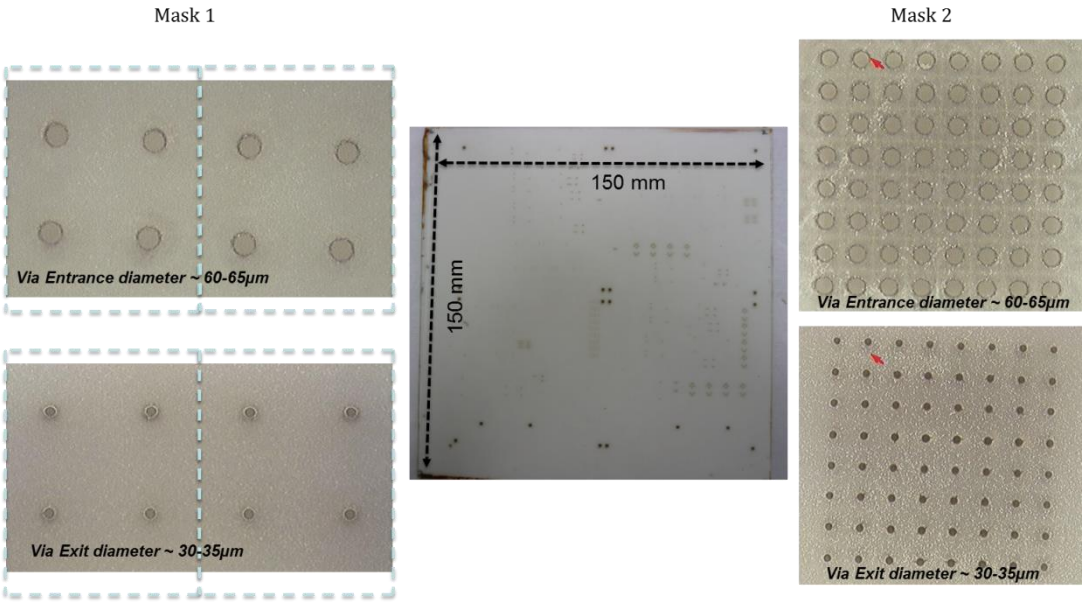


Figure 115: TPV formation in polymer laminated glass panel using two different mask patterns.

After TPV formation, a semi-additive plating (SAP) approach was used to simultaneously metallize the RDL and TPVs with a target copper thickness of 8-10µm. First, a permanganate-based chemical desmear process was used to treat the polymer surface and the TPV sidewalls. Electroless copper deposition was then used to deposit a thin conductive layer (100-300 nm). A 15µm thin dry-film negative photo-resist (PR) was laminated for patterning using photolithography. Electrolytic plating was used to achieve a final copper thickness of approximately 8-10µm. A snapshot of the sample at different stages of processing is shown Figure 116.

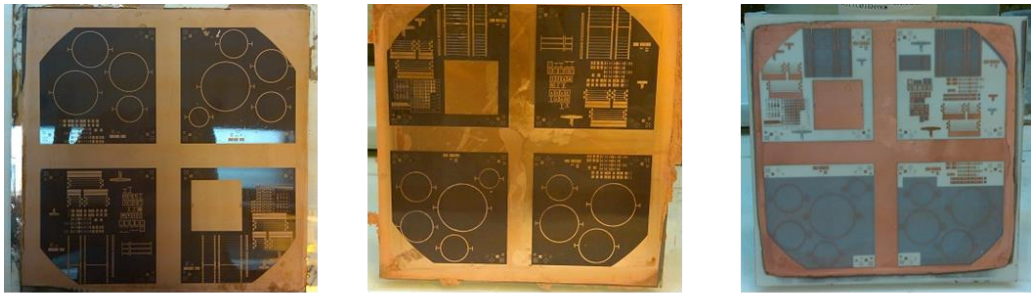


Figure 116: Two metal layer glass interposer fabrication: a) after PR lithography, b) after electrolytic plating, c) after PR and seed layer removal - 2 metal layer interposer.

After completing the two metal layer stack-up, build-up layers were fabricated using ZIF as the polymer material. The schematic process flow used to achieve four metal layer structures is illustrated in Figure 117. Initially, the copper on the core layers were treated with bond-film solution to roughen the copper surface and provide good adhesion between the metallization and the build-up polymer material (ZIF). Next, a double side lamination process was used to form the ZIF build-up layer. Lamination of ZIF consisted of two steps, a) vacuum lamination and b) hot-press. The use of vacuum ensured void-free lamination, especially inside the conformally metallized glass TPVs. Subsequently, hot-press lamination was carried out to planarize the polymer surface. The ZIF sample was cured in an oven at 180^{o}C for 30 minutes.

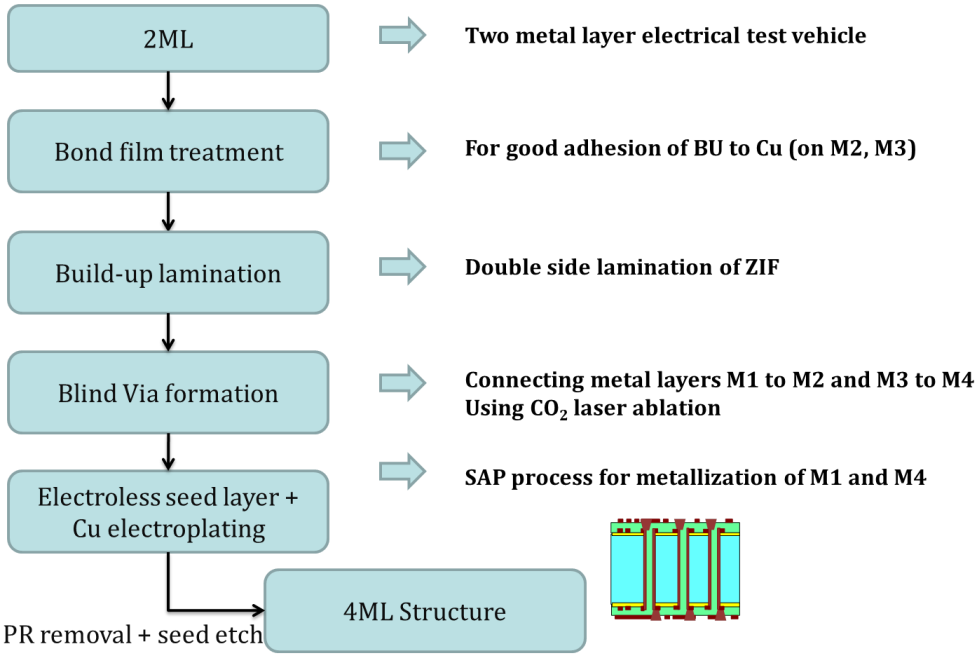


Figure 117: Process flow schematic for four-metal layer fabrication.

The temperature profile used for curing the ZIF polymer is shown in Figure 118.

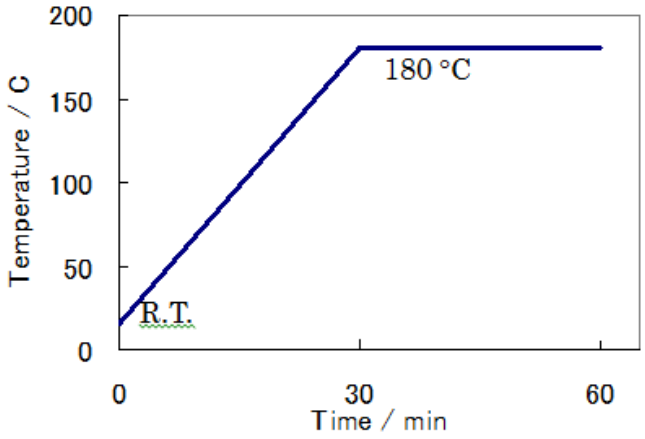


Figure 118: Temperature profile of ZIF curing process.

The process parameters used in the two-stage ZIF lamination process are summarized in Table 11.

Table 11: Process parameter for ZIF lamination

Process	Temperature	Pressure	Duration
Vacuum lamination	200 F	-	10 sec
Hot press	248 F	60-90 psi	90 sec

After ZIF lamination, micro-vias were formed (using CO_2 lasers) in the ZIF layer to connect the bottom metal layers to the top-most metal traces. An optical cross-section image of micro-vias in build-up is shown in Figure 119. The diameter of the micro-vias depends on the wavelength of incident radiation. The use of a CO_2 laser helped achieve via diameters between 30-35µm through a ZIF polymer with a thickness of 17µm. Excimer lasers could be used to form smaller micro-vias on the build-up layer.

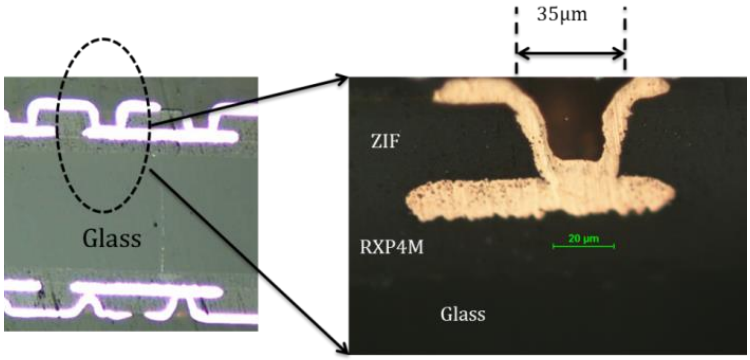


Figure 119: Cross-section image of micro-vias formed in the build-up layer using CO_2 laser ablation.

The SAP process was repeated to achieve a four-metal layer stack-up. An optical image of the glass panel after four-metal layer fabrication is shown in Figure 120. Some of the structures fabricated on the M1 layer like the micro-strip lines (MSL), planar spiral inductors, and daisy chain patterns for the TPV reliability study are also illustrated in Figure 120.

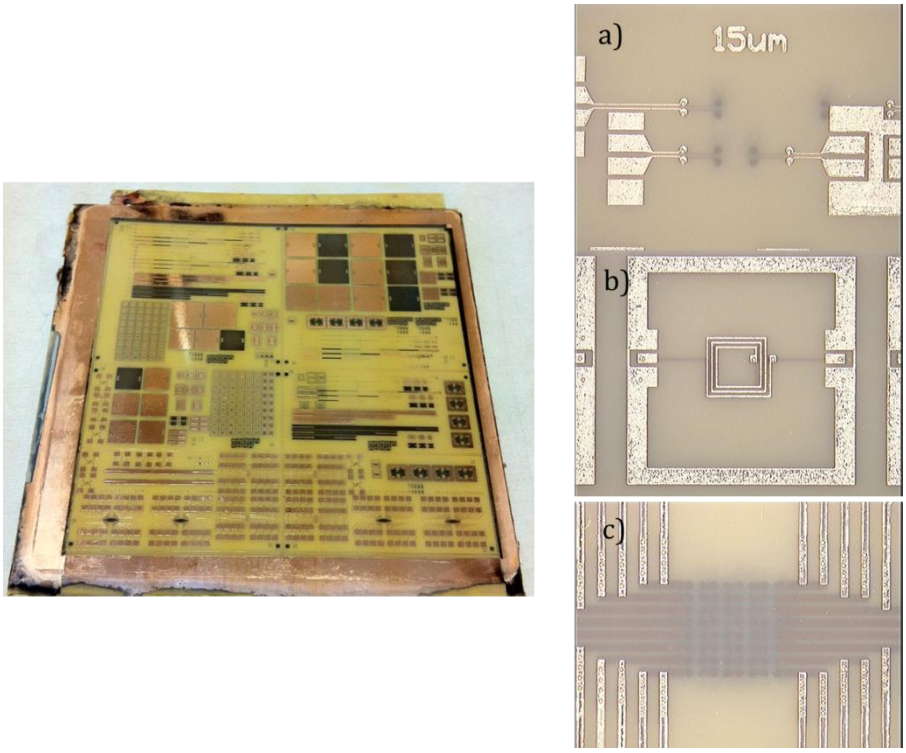


Figure 120: Optical image of test vehicle after four-metal layer fabrication, showing structures on M1 layer: a) MSL line, b) Inductor, c) TPV daisy chain.

A detailed cross-section study was performed on the fabricated samples to observe the interfaces and to investigate copper metallization inside the TPVs. The optical and SEM cross-section image of the four-metal layer stack-up with via transition is illustrated in Figures 121-123.

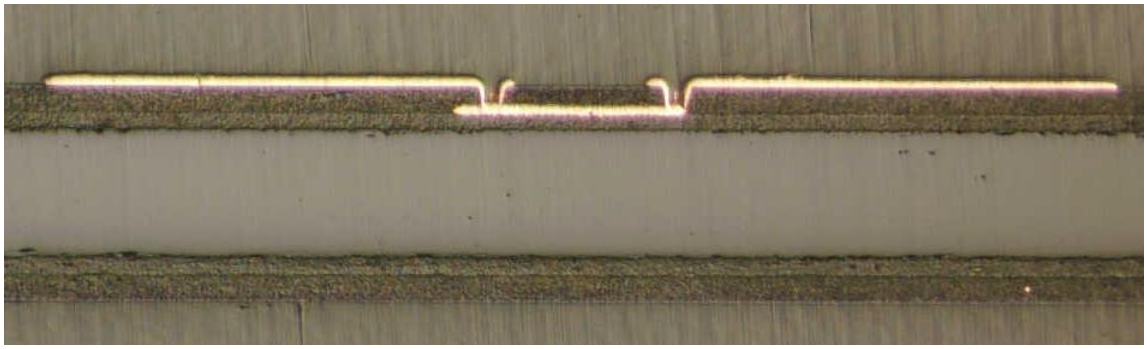


Figure 121: Cross-section image of transmission line across two-metal layers, connected with micro-vias.

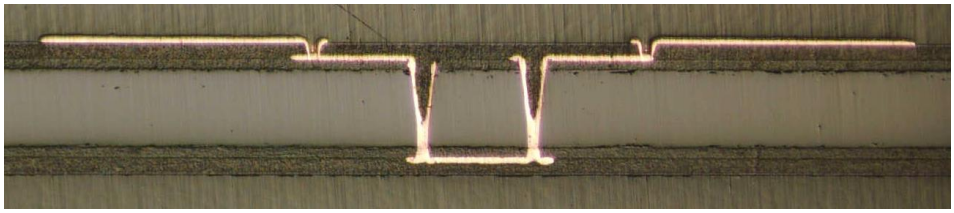


Figure 122: Cross-section image of transmission line across three layers, connected with TPVs and micro-vias.

The basic four-metal layer process flow and stack-up with TPVs shown in Figure 123 can be used to design interposer packages for mobile or high-performance applications.

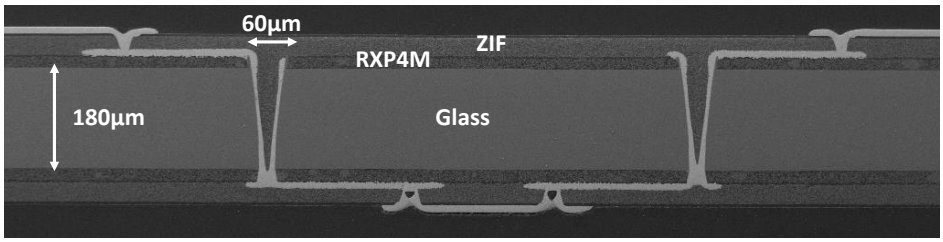


Figure 123: SEM Cross-section image of four-metal layer glass interposer structure with TPVs.

6.2 RF Filters on Glass

Glass is an ideal material for RF applications due to its excellent dimensional stability, surface flatness, and low-loss. In addition, it is possible to design passive devices with high 'Q' factors on glass substrates. This section will describe the materials and processes required to fabricate multi-layer glass interposers with TPVs.

A filter is a component within a RF circuit that allows specific frequencies to pass through the circuit while it attenuates the undesired frequency components. Based on the desired frequency band, filters can be designed to have either 'high-pass', 'low-pass' or 'band-pass' responses. There are two basic requirements for a filter: a) very low insertion loss in the pass-band and b) high attenuation in the stop band. Such filters are commonly designed using RLC resonance circuits. By using semiconductor tools and process technologies, it is possible to fabricate passive RLC components on silicon, glass or LTCC (low-temperature-co-fired-ceramic) substrates, leading to an

integrated passive device (IPD) module [109, 110]. However, traditional IPDs on glass are limited to single-side components due to wafer-based process methods. By using the methods developed in this research to fabricate small-pitch through vias in glass (TPVs), and a panel-based process approach, significant reduction in form-factors of RF IPDs can be achieved from double-side components. In fact Sridharan et.al have investigated such double-side glass interposers and studied the use of TPVs as via-based inductors [90]. The study focused on band-pass-filters having a center frequency of 2.4 GHz and 5.3 GHz respectively. The filters were designed using stitched capacitors and via-based inductors, and the measured insertion loss was observed to be less than 2dB with 35dB out of band rejection.

In this research, the work done by Sridharan is extended to thinner glass with smaller TPVs and describes the design, fabrication and electrical characterization of low pass filters (LPFs) on double-side glass interposer. A schematic cross-section of the four-metal layer RF filter module is shown in Figure 124. The glass substrate has a thickness of 100µm, and has TPVs with an entrance diameter of 60µm at 120µm pitch. ZIF is used as the polymer on glass and also as the build-up polymer material. The stack-up consists of four metal layers (two metal layers each on the top and bottom side).

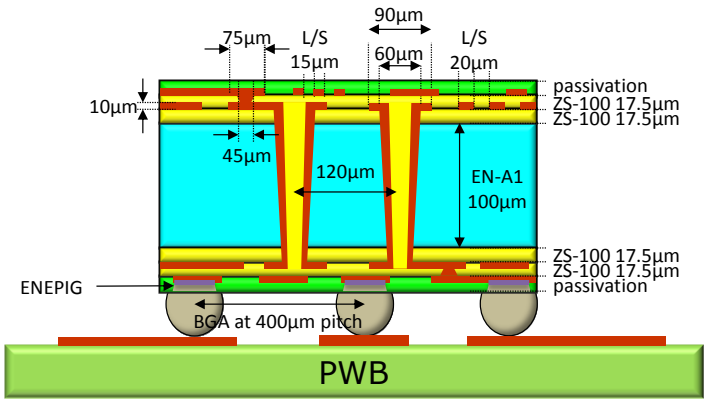


Figure 124: Schematic cross-section of four-metal layer RF filter module [111, 112].

Four LPFs were designed at 0.8 GHz, 1.79 GHz, 2.5 GHz and 5.3 GHz using LC resonance circuit. The circuit diagram is shown in Figure 125. Each filter was designed using two metal layers on one side of the interposer. Interconnection between the top and bottom filters or other circuit components was achieved using TPVs. The inductors comprised of planar spiral coils, and the parallel-plate capacitors were designed on the build-up layer to achieve higher capacitance density.

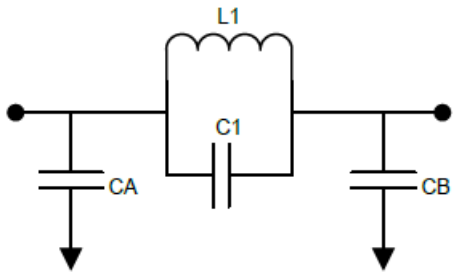


Figure 125: Circuit schematic for low pass filters.

The process flow schematic for the four-metal layer LPF device is shown in Figure 126. The materials and process sequence are similar to those explained in the previous section. However, as the schematic indicates, the following three additional steps were included to complete the RF module fabrication: a) lamination of passivation layer and patterning, b) electroless nickel-palladium-gold (ENEPIG) surface finish, and c) device singulation and board level assembly.

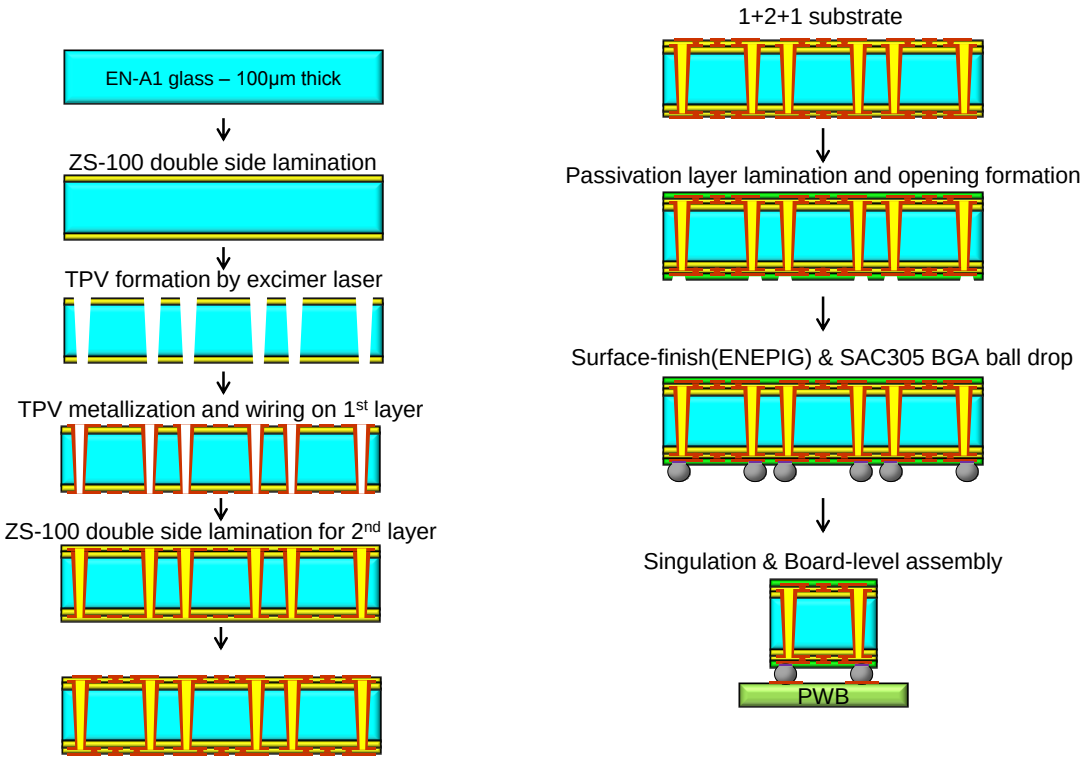
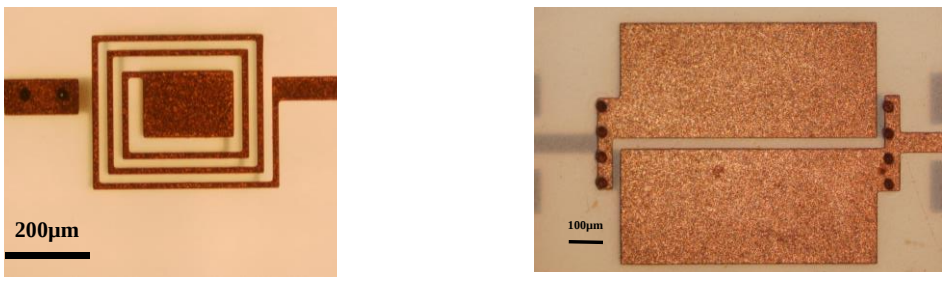


Figure 126: Process flow schematic, showing four-metal layer RF demonstrator fabrication.

An optical image of the fabricated passive structures, namely: spiral inductors and parallel-plate stitched capacitors are shown in Figure 127. Further, the top view image of the fabricated filter devices is shown in Figure 128.



(a) (b)

Figure 127: Optical image of fabricated structures: a) spiral inductors and b) parallel-plate stitched capacitors.

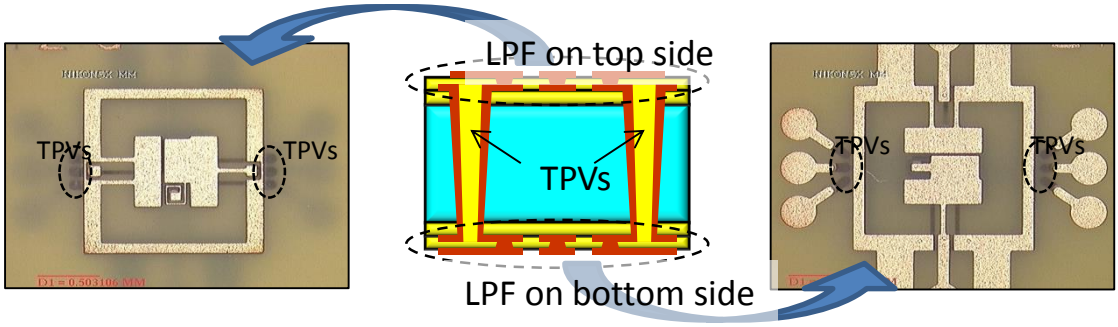


Figure 128: Top view image of fabricated filters on double side glass interposer.

A vector-network-analyzer was used to perform high frequency measurements on the fabricated LPFs. Initially, the filter response was measured at the panel-level after four-metal layer fabrication and prior to passivation and BGA attach (Figure 129). This measurement helped identify the filters that were electrically functional.

Figure 129: High frequency measurements at the panel level.

Short-open-load-through (SOLT) calibration was performed prior to actual measurement using ground-signal-ground (GSG) probes having a probe pitch of 500µm. The measured LPF response of the 800MHz filters on the top and bottom side of the glass interposer is shown in Figure 130. The measured insertion loss was less than 1dB with high rejection in the stop band (> 20dB). A good model to hardware correlation was observed in the case of LPFs operating in all the frequency bands (0.8 – 5.3GHz).

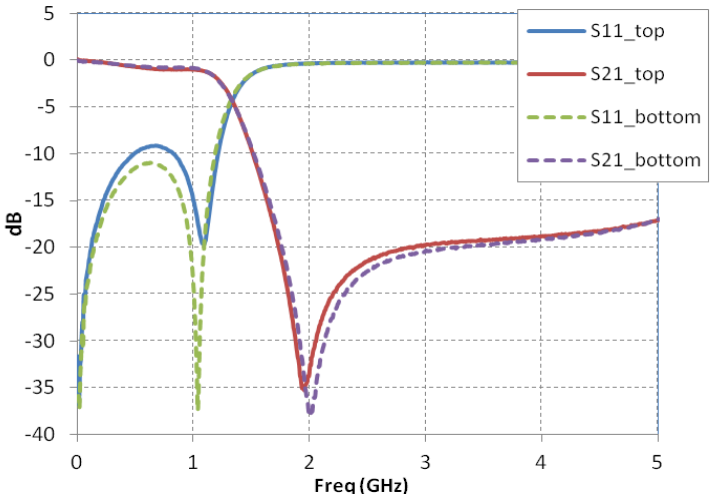


Figure 130: Measured response of top and bottom side LPFs (0.8 GHz).

A comparison between measured and simulated response of the LPFs in the different frequency bands is provided in Table 12. A slight difference between simulation and measurements can be attributed to TPV parasitics and slight variations in the inductor and capacitor values caused due to process variations. A snapshot of the RF device after assembly onto the PWB is shown in Figure 131.

Table 12: Comparison between measured and simulated response

Sim f_c	0.85	1.79	2.5	5.3
Measured	0.98	2.03	2.82	5.72
Δf_c (%)	15.3	13.1	12.9	7.9
IL @ f_c	0.91	0.77	1.1	0.93
ΔIL (%)	82.5	70.9	29.1	69.5
RL @ f_c	17.4	35.8	21.4	32.3
ΔRL (%)	-30	55.7	7.07	15.5

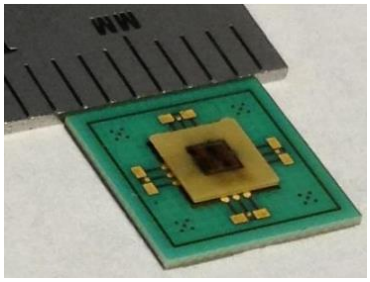


Figure 131: Glass interposer based RF module after assembly onto PWB.

A cross-section examination was performed on the structure after board level assembly and the image obtained is shown in Figure 132.

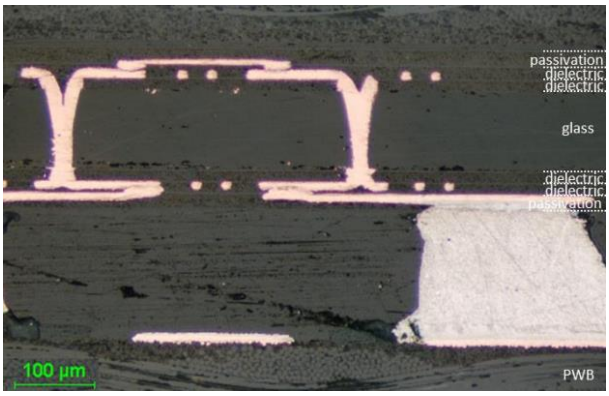


Figure 132: Cross-section image of RF module, showing BGA connections to the PWB.

The assembled interposers were subjected to electrical characterization at the board-level as shown in Figure 133.

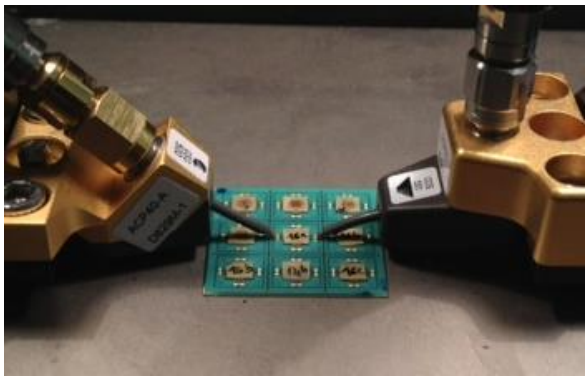


Figure 133: Board level measurement of LPF.

The measured S-parameter response of a 2.5GHz LPF is shown in Figure 134. Overall, the measurement results from VNA characterization corroborated well with the simulated results. The low-loss of glass resulted in low insertion loss. Additionally, the ability to use small TPVs in thin-glass interposers helped achieve significant reduction in form-factor of the final LPF device. The size of a single LPF is a function of the operating frequency, and the designs implemented in this research work had an X-Y size ranging from 0.8mm (for 5.3 GHz filter) to 2mm (for 800 MHz filter).

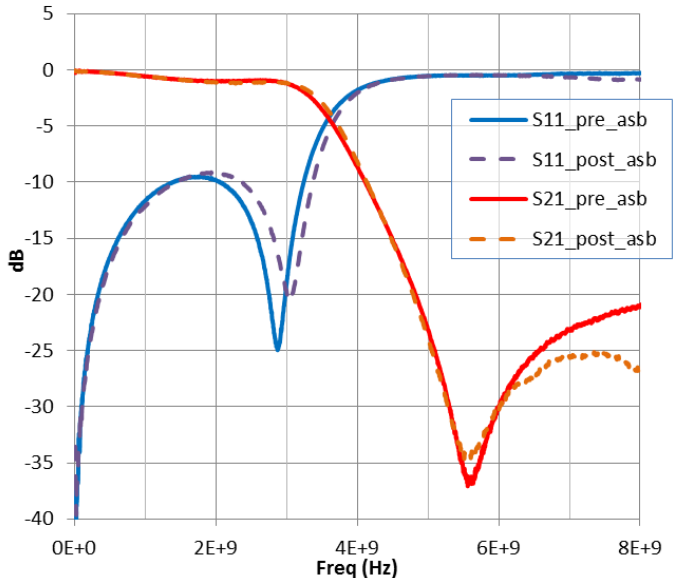


Figure 134: Measured LPF (2.5GHz) response before and after assembly onto PWB.

6.3 Electrical Characterization of TPVs in ultra-thin (30µm) glass interposers

a) Test vehicle-design

To demonstrate the feasibility of the proposed ultra-thin glass interposer with small TPVs, an electrical test-vehicle was designed, fabricated, and electrically characterized using high frequency RF probes and a vector network analyzer (VNA). As shown in Figure 135, the test vehicle design consisted of transmission line structures, namely, coplanar waveguides (CPW) and micro-strip lines (MSL) with TPV transitions. In addition to the transmission lines, passive circuits like spiral inductors and parallel-plate capacitors were also designed and fabricated on both sides of the ultra-thin glass substrate.

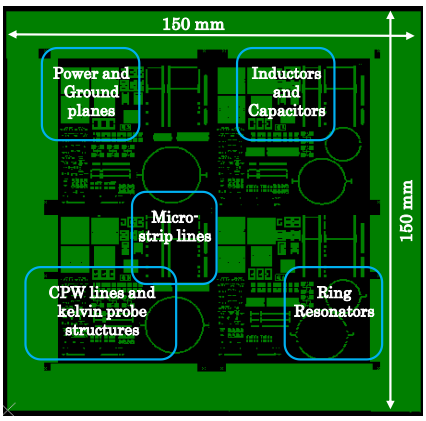


Figure 135: Test-vehicle design (150mm x 150mm) showing layout of top metal layer.

b) Test-vehicle fabrication

To fabricate the two-metal layer glass interposer, a panel-based double-side process approach identical to the process described in the first part of this chapter was used (Figure 136). The thickness of the glass substrate was 30µm, and the ZIF thickness was 17µm.

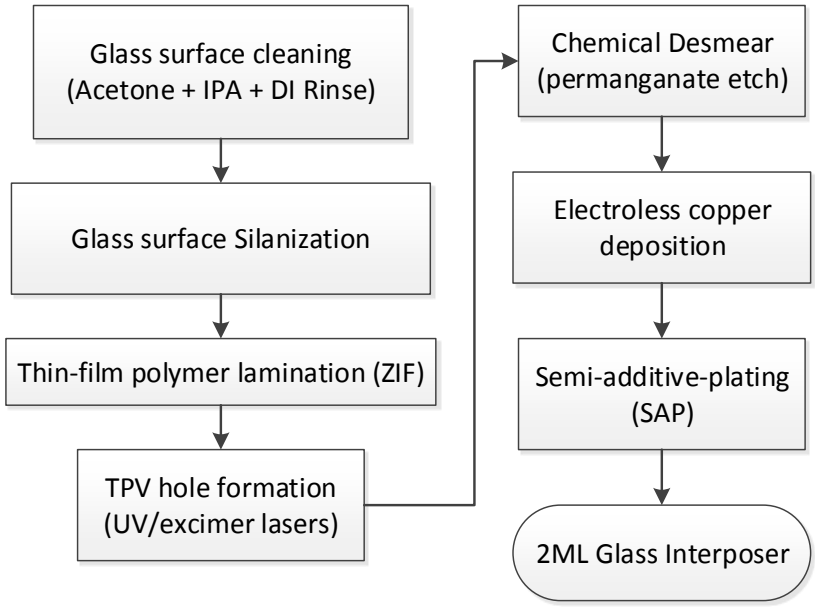
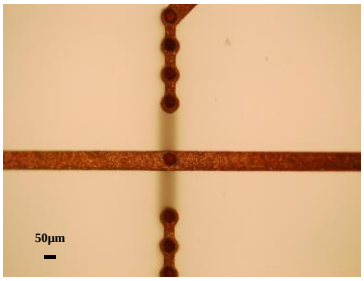
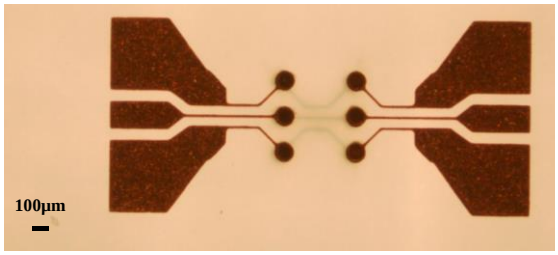


Figure 136: Process flow for 2-metal layer glass interposer fabrication.

An optical image of the fabricated test structures is shown in Figure 137 and a snapshot image of the ultra-thin glass panel after fabrication is shown in Figure 138. The use of thin-polymer layers on glass helped achieve defect-free handling of glass even at a thickness of 30µm.





(a) (b)

Figure 137: Fabricated electrical test structures: a) Kelvin probe structure for TPV resistance extraction, and b) Coplanar waveguide.

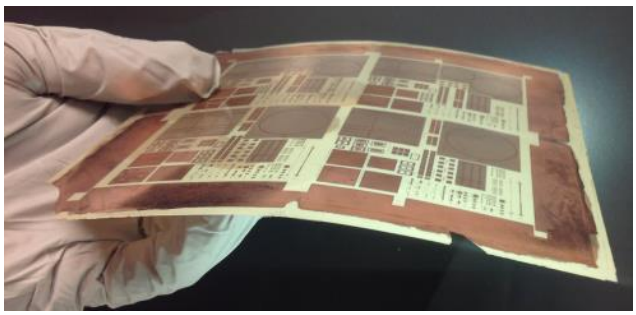


Figure 138: Two-metal layer prototype demonstrator.

A detailed cross-sectional examination was carried out after fabricating the two-metal layer interposer. A SEM cross-section image of CPW line with via transition is shown in Figure 139. Via diameter on the entrance (~30µm) and exit side (~15µm) of the TPVs in glass was observed to be relatively smaller compared to the openings (40µm entrance/20µm exit) in the polymer. This can be attributed to excess ablation of polymer during the laser process. The use of a thinner polymer layer could help minimize excess ablation, thereby leading to similar via openings in both polymer and glass.

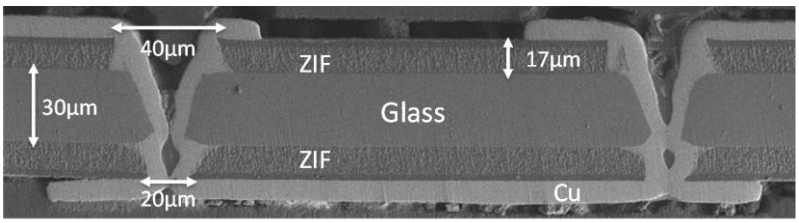


Figure 139: Cross-section SEM of 2-metal layer electrical test vehicle.

Test vehicle characterization – Electrical characterization of TPVs

The electrical characterization of TPVs in 30µm thin glass is divided into two parts: a) DC measurements and b) high frequency RF characterization.

6.3.1 DC measurements

Four-point kelvin probe structures were designed to characterize the DC resistance of TPVs. The DC resistance (R) of a conformal plated TPV was theoretically computed using the following equation:

$$R = \int_0^h \left(\frac{\rho_{cu}}{2t_{cu}.\pi \left[\frac{(a-b)x}{h} + b - 0.5t_{cu} \right]} \right) . dx \qquad (19)$$

The terms t_{cu} and ρ_{cu} correspond to the thickness of the conformal metal and resistivity of copper respectively while ‘a’ and ‘b’ represent the radii of exit and entrance side of TPV. The value of ‘h’ indicates the total height of the TPV, which is 64µm for the fabricated test vehicle. Theoretical TPV resistance was calculated using Equation 19 with the following values: a = 10 µm, b = 20 µm, h = 64 µm, t_{cu} = 8 µm and ρ_{cu} = 1.72 x 10^{-2} Ωµm.

The above formula for TPV resistance was derived by assuming the TPV to be a perfect cone. Thus, a two dimensional projection of a TPV has a shape of a trapezium as shown in Figure 140. The radii on the entrance and exit side of the TPV are ‘b’ and ‘a’ respectively and r_1 is the outer radius of the TPV at a distance of x from the TPV entrance.

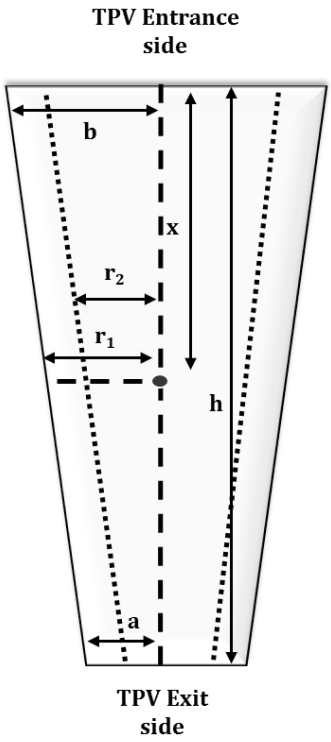


Figure 140: 2D representation of TPV.

Based on the geometry shown in Figure 140, the following relation can be obtained:

$$\frac{b - r_1}{x} = \frac{b - a}{h} \tag{20}$$

$$r_1 = \frac{(a - b)x}{h} + b \tag{21}$$

The metallization thickness (t_{cu}) is defined as ($r_1 - r_2$), wherein r_1 and r_2 are the outer and inner radii across the conformal metallization. The TPV is assumed to have conformal metallization throughout its cross-section. The cross-section area for such a TPV can be written as: $\pi\,(r_1 + r_2)t_{cu}$. The resistance of the TPV can be derived by integrating over the entire length 'h'.

$$R = \int_0^h \frac{\rho_{cu}}{\pi(r_1 + r_2)t_{cu}}\,dx \tag{22}$$

Substituting the values for r_1 and r_2 in the above equation:

$$R = \int_0^h \frac{\rho_{cu}}{\pi\left(\frac{(a-b)x}{h} + b + r_1 - t_{cu}\right)t_{cu}}dx \tag{23}$$

$$R = \int_0^h \frac{\rho_{cu}}{\pi\left(2\frac{(a-b)x}{h} + 2b - t_{cu}\right)t_{cu}}dx \tag{24}$$

$$R = \int_0^h \frac{\rho_{cu}}{2\pi t_{cu}\left(\frac{(a-b)x}{h} + b - 0.5t_{cu}\right)}dx \tag{25}$$

The above expression is the same as equation 19.

The TPV resistance of the metallized vias in 30 µm thin glass was measured using 4-point kelvin probes. Such a measurement using kelvin probes helps to accurately determine the resistance of a single TPV by eliminating the resistances of the connecting wires. A circuit schematic of the four-point kelvin structure is shown in Figure 141.

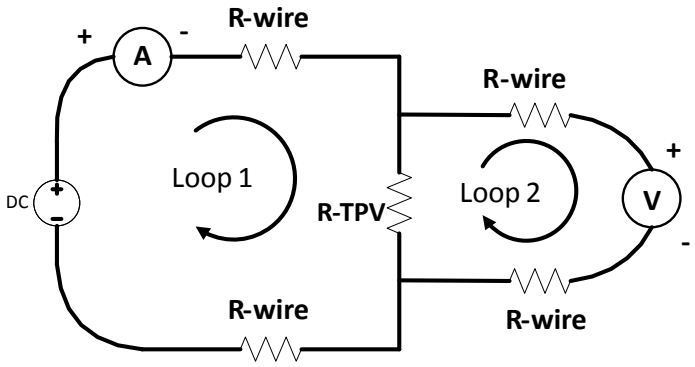


Figure 141: Circuit Schematic of Four-point Kelvin probe.

As shown in Figure 141, an ammeter and voltmeter was used to measure the current and voltage across the TPV. Due to the very high resistance of the voltmeter (V), the current through loop 2 is negligible, and almost all the current flows through loop 1. This current through loop 1 was measured using an ammeter (A). Finally, the resistance of the TPV was computed using ohms law (R = V/I). The four-probe measurement helped eliminate the resistance of the wires and the DC resistance of a single TPV was determined.

The results obtained from theoretical calculation and experimental measurements are summarized in Table 13. The observed variation between the theoretical and measured resistances (2.14 and 2.92 ± 0.52 respectively) can be attributed to the following two reasons: a) the theoretical calculation assumes the TPV to be a perfect cone, but based on the study on via formation, it was observed that the processed via geometry deviates from a perfect conical structure; and b) the value 'h' assumed in the formula is 64µm, which does not capture the effect of the via pads. The difference between the theoretical and measured values can be minimized by adding the TPV pad resistance to the theoretical value. For the calculation of pad resistance, a conformal metallization was assumed, leading to annular disc geometry for via pad, and the formula: $R^* = \rho.\frac{l}{\pi(r_1+r_2).t_{cu}}$ was used to compute the pad resistance, where r_1 and r_2 are the outer and inner radii of the annular disc, and t_{cu} is the thickness of the conformal metal.

Table 13: Theoretical and experimental values of TPV resistance

Parameter	Theoretical (mΩ)	Theoretical resistance value of TPV pads (2R*) (mΩ)	Measured (mΩ)
Resistance	2.14	Approx. 0.4 (assuming r_1 = 20µm; r_2 = 10µm, l = 10µm and t_{cu} = 10µm)	2.92 ± 0.52

6.3.2 High frequency RF measurements

Electrical characterization of the two-metal layer ultra-thin glass interposer was carried out using a vector-network-analyzer (VNA) and high frequency RF probes. Short-open-load-through (SOLT) calibration was performed on the measurement set-up followed by S-parameter measurements on the individual test coupons using 250µm pitch GSG probes. The insertion loss of the two major

components of interposers, namely redistribution lines (RDLs) and through-package-vias (TPVs) are presented.

In the case of CPW lines (RDLs) in glass, a good correlation trend was observed between the measured and simulated insertion-loss parameter. The total length of the CPW line was 6.2mm, while the line width and spacing were 120µm and 18µm respectively. The simulated and measured insertion loss (S12) is shown in Figure 142.

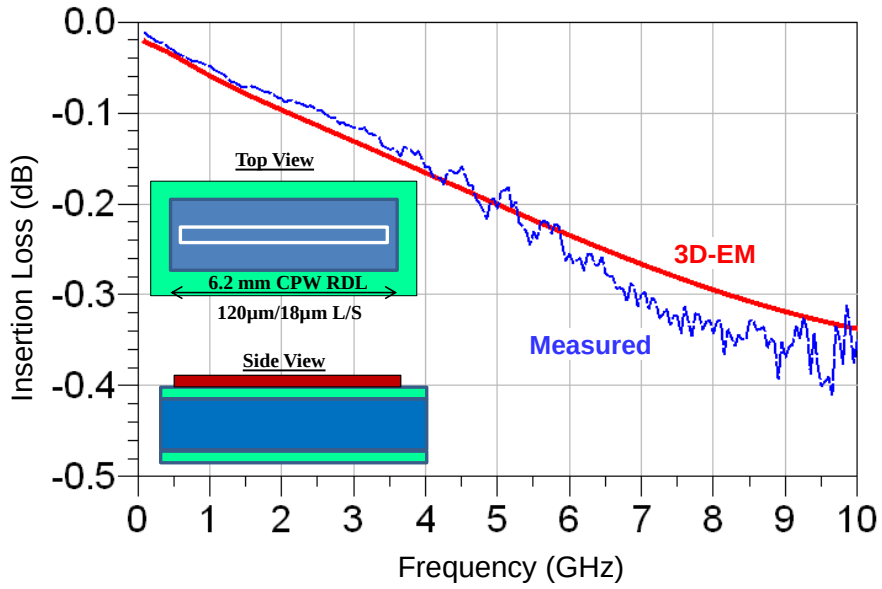


Figure 142: Measured insertion loss (S_{12}) of Glass interposer RDL traces.

The effects of combining signal lines with TPVs were then studied to analyze the impact of ultra-fine pitch glass vias on signal performance. Impedance matched CPW line structures containing 1mm RDL of 120µm line width and 20µm spacing were measured with and without TPV as shown in Figure 143. The interconnection showed extremely low signal loss (around 0.1 dB) up to 20GHz with a good correlation trend between the measured and simulated insertion-losses. However, some minor variations between the simulated and measured results were observed due to the challenges associated with low-loss microwave calibration.

As illustrated in Figure 143, overall, it was observed that glass interposers exhibit superior signal performance because of the very high resistivity of glass and

reduced return loss due to shorter via length, leading to overall lower TPV and RDL insertion loss.

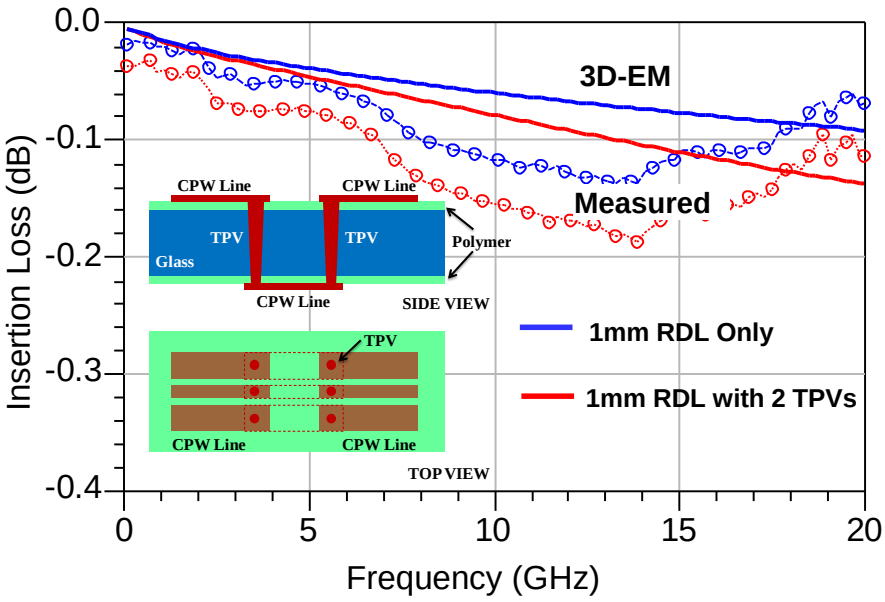


Figure 143: Measured insertion loss (S_{12}) of CPW line with TPV transitions.

Chapter 7

RESEARCH SUMMARY AND CONCLUSIONS

This research is a first systematic and fundamental approach to exploring glass as an electronic substrate. To meet the increasing demand for high bandwidth beyond POP, ultra-thin 3D glass interposers with small-pitch TPVs are proposed and demonstrated as a compelling alternative to 3D IC stacks interconnected with TSVs. In the 3D glass interposer approach, high-bandwidth and short interconnections between logic and memory ICs are achieved using ultra-small pitch TPVs in ultra-thin glass substrates. Although glass, as an electronic interposer exhibits many benefits, the brittleness of glass gives rise to two fundamental challenges that have been identified as: a) small-via hole formation at small-pitch with minimum surface damage and b) copper metallization of these holes with good adhesion and thermo-mechanical reliability.

To address the aforementioned scientific challenges, a systematic study was undertaken to provide a fundamental understanding of how these challenges could be overcome to allow the development of reliable small-pitch TPVs in ultra-thin glass interposers. A simple process flow is shown in Figure 144 that illustrates the scope of research tasks and the key scientific and engineering contributions resulting from each task. As shown in this figure, the systematic study was divided into four main tasks: a) electrical modeling and design of TPVs, b) TPV hole formation, c) TPV metallization and thermo-mechanical reliability analysis, and d) TPV electrical characterization and demonstration of 30µm thin-glass test vehicle with small TPVs.

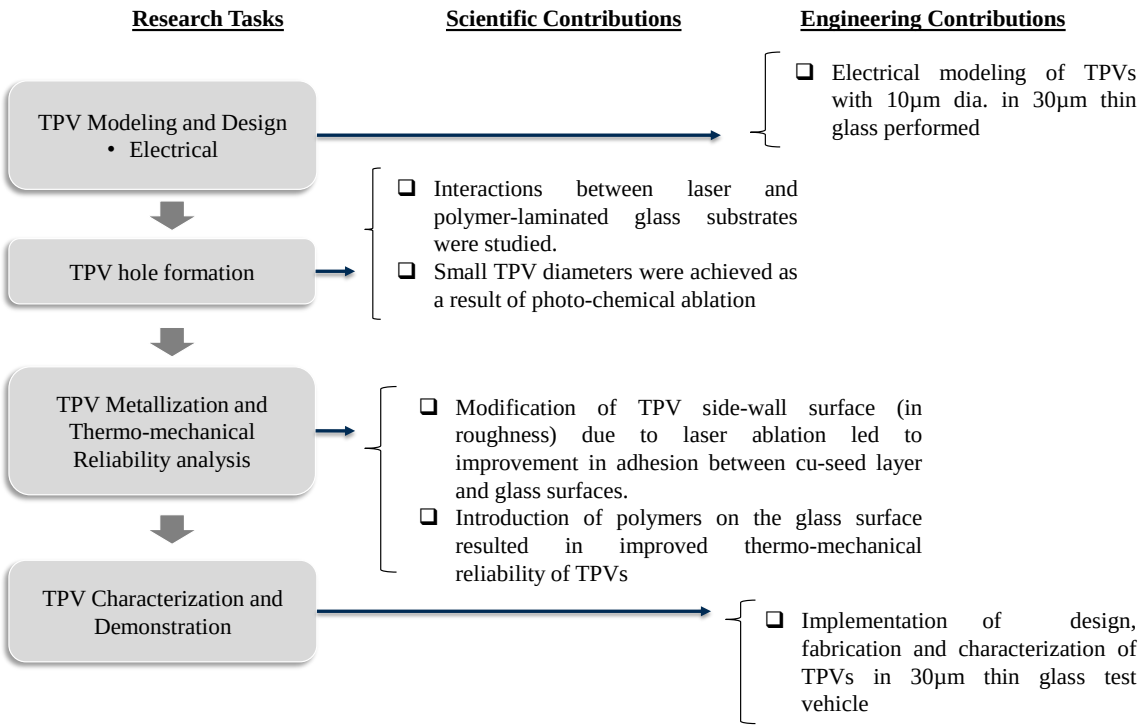


Figure 144: Research tasks and key scientific and engineering contributions.

The research results and analysis of each research task were documented and discussed in separate chapters within this document. The following section provides a summary of the key findings of each research task.

7.1 Research Summary:

7.1.1 Electrical Modeling and Design of ultra-small TPVs in glass

- TPVs in glass with an entrance diameter of 10-15µm at 30µm pitch were modelled using 3D full wave EM solver (HFSS). It was observed that the insertion loss and cross-talk values of TPVs in glass were significantly lower compared to TSVs in Si. The vias in glass showed insertion loss values less than 0.05dB till 40GHz and isolation greater than 37dB between vias (cross-talk). On the other hand, TSVs with similar dimensions showed more than 0.3dB loss at 20GHz and an isolation of about 30dB (cross-talk).

- Additionally, a parametric study was performed by changing the electrical properties of materials within the 3D model. The following variations were considered for the parametric study: a) change in glass material composition, resulting in variations in dielectric constant and loss tangent values of glass; b) change in conductor material inside TPVs, causing variation in TPV resistivity; and c) change in metallization thickness. The study showed that the frequency response of the TPVs was not affected by changes in the metallization thickness or variation of glass material. However, a slight change in the S-parameter response was observed between the different metallization materials. The study revealed that copper is highly favorable for achieving the best electrical performance.

7.1.2 TPV Hole Formation

- First, a detailed study on glass machining methods and their mechanism was undertaken. Next, several TPV formation methods were explored, including mechanical processing, photo-via formation, and laser ablation, to achieve the smallest TPV diameter with minimum damage around the via. A detailed study on laser ablation in glass using different laser systems (UV, CO_2, excimer, pico-second) was carried out. The study showed that the smallest via diameters (30µm diameter in 180µm thin glass) with minimum thermal and mechanical damage around the TPV can be achieved using 193nm ArF-based excimer lasers. The small diameter of TPVs was attributed to the small spot size of the laser beam, and the photo-chemical nature of the ablation process that resulted in minimum damage during TPV formation.

- To achieve smaller TPV diameters (< 30μm) similar to TSVs in Si, ultra-thin glass substrates with thicknesses less than 100μm were explored. Thin glass, however, is prone to brittle failure, and thus to achieve crack-free glass handling during TPV processing, novel thin-film polymers (RXP4M and ZIF) were laminated on the glass surface.
- Next, a combination of thin glass substrates (30-50μm) and excimer laser ablation (193nm) were investigated to achieve ultra-small via holes.
- In addition to the formation of small TPVs, the through-put capability of excimer laser ablation process was studied. The measured through-put values of excimer lasers (193nm and 248nm) were compared with CO_2 laser. TPV through-put values in the range of few hundred vias per second (400-1000 vias/ second) were achieved using projection-based ArF and KrF laser systems. However, the laser field size was reduced to 1mm x 1mm, to ensure higher laser fluence, which is well beyond the threshold value for glass ablation. Thus, the findings revealed that a step and repeat approach is required to form through holes over a larger panel size.

7.1.3 TPV Metallization and Thermo-mechanical Reliability Analysis

Because laser ablation in ultra-thin glass substrates resulted in small-pitch TPVs, a double-side process approach could be implemented to metallize the TPVs. This double-side approach is a unique feature of this research study and is different from metallization of TSVs in silicon. The processing of glass can be done on both-sides simultaneously without the need for CMP.

A. Metallization

- To apply electroless copper deposition, polymer-laminated glass substrates with TPVs were initially subjected to chemical desmear using permanganate solution

to improve the adhesion between seed-layer and polymer. A combination of electroless and electrolytic copper plating was used to metallize the TPVs with entrance and exit diameters of 15µm and 8µm respectively in 30µm thin glass. Logically, a reduction in glass thickness could potentially improve the through-put of via plating process by significantly reducing the plating time.

- The side-wall of TPVs formed by excimer laser ablation showed a thin layer of re-deposited glass. The mechanical property of this layer was analyzed using nano-indentation tests. The tests revealed that the re-deposited glass exhibits intermediate mechanical behavior between that of bulk glass and polymer.

B. Thermo-mechanical Reliability Analysis

- Preliminary reliability tests were performed on TPV daisy chains in polymer laminated glass substrates. TPV daisy chains were subjected to thermal cycling between -55^{o}C to 125^{o}C and showed stable daisy values up to 1500 thermal cycles. Micro-structural and X-ray examinations after TCT did not reveal any cracks or delamination from the TPV side-wall.
- Thin polymer layers laminated on the glass surfaces act as a stress buffers, especially in the high-stress concentration regions (TPV edges). Because the polymer exhibits relatively lower modulus values compared with glass or copper, most of the stresses at the copper-polymer or copper-polymer-glass interfaces are converted into strain in polymer.

7.1.4 TPV Characterization and Demonstration

A. Characterization

- To study the electrical behavior of small TPVs, and to validate the results from electrical simulations, a test vehicle using 30µm thin glass was designed and

fabricated using panel-based, double-side processes. The design comprised of transmission lines and kelvin probe structures.

- Both the DC as well as high frequency characteristics of TPVs in glass were analyzed through measurements. A stable DC resistance value of 2.9mΩ was measured for a single TPV. The result obtained was in good agreement with the theoretically- predicted value. Next, high frequency RF probes were used to obtain the s-parameter response of TPVs in thin glass. The measured insertion loss of transmission lines with TPVs was observed to be significantly lower (0.1 dB till 20GHz) compared to TSVs in Si, owing to the high resistivity of glass and the absence of capacitance due to oxide liner.

B. Demonstration

- An innovative process-flow was developed for fabricating multi-layer glass interposers using 100-180µm thick glass substrates. The RDL stack-up consisted of four metal layers with RXP4M as the dielectric on the core and ZIF as the build-up polymer. The metal layers across the build-up layers were connected using micro-vias, while the TPVs provided electrical connection between metal layers on both sides of the glass substrate. The entrance and exit diameters of TPVs achieved using excimer laser ablation were 60µm and 35µm respectively.
- Once the process-flow for multi-layer glass interposers with TPVs was established, four low-pass filters (LPF) with cut-off frequency values between 0.8 and 5.2 GHz were fabricated within the four–metal layers on the glass interposer. A good correlation between the simulated and measured value of insertion loss was obtained. The filters exhibited very low insertion loss (< 0.1 dB) in the pass band and a high rejection in the stop band (> 20 dB).

7.2 Key contributions

A. Scientific Contributions

- The formation of small TPV holes at small pitch with minimum defects was studied using photo-thermal and photo-chemical mechanisms.
- The interactions between laser and polymer-laminated glass substrates were studied. It was observed that lower wavelength excimer lasers helped achieve small TPV diameters due to their smaller spot size and photo-chemical nature of the ablation process. The TPVs formed have a diameter of 10µm at 30µm pitch in glass substrates having a thickness of 30µm.
- Detailed analysis of TPV cross-sections revealed thin layer of re-deposited glass. This modification of TPV side-wall surface (in roughness) led to improvement in adhesion between cu-seed layer and glass surfaces.
- The introduction of polymers on the glass surfaces helped minimize the thermo-mechanical stresses inside TPVs, leading to improved reliability.

B. Engineering Contributions

- Electrical modeling and design of ultra-small TPVs (10-15µm diameter) in ultra-thin glass substrates (30µm) was performed.
- Based on the fundamental understanding of TPV formation and their metallization, the design, fabrication and characterization of 30µm thin glass test-vehicle (two-metal layer) was implemented.
- An innovative process-flow was developed for fabricating four-metal layer glass interposers.
- Miniaturized RF filter designs were implemented in four-metal layer glass interposers. The characterization results showed very low-insertion loss with excellent model to hardware correlation.

7.3 Future Extensions

This dissertation explored ultra-thin glass based interposers and focused on addressing the fundamental challenge associated with TPV hole formation and their metallization. The following studies are proposed as future extensions of this research:

a) TPV Formation:

Via formation using laser ablation resulted in a tapered via. However, for high performance applications a vertical via profile may be desirable. Thus, fundamental studies can be undertaken for achieving vertical TPV holes in glass. Additionally, through-put enhancement techniques for via hole formation can be investigated.

b) TPV metallization and reliability:

This study identified the presence of a thin layer of re-deposited material along the side-wall of TPVs. An initial characterization of the mechanical property of this material was conducted. A more comprehensive study can be undertaken to ascertain the chemical and mechanical behavior of this re-deposited material on the side-wall of TPVs and correlate its impact on TPV reliability.

The thermo-mechanical reliability of TPVs in glass is a major concern, and therefore, a more detailed and exhaustive study on reliability and failure analysis of metallized TPVs can be undertaken. This research studied novel-polymer dielectrics on smooth glass surface to achieve metallized through holes. Direct metallization of copper on the glass surface still remains a significant challenge and further study is required to achieve reliable TPVs in bare glass substrates without intermediate dielectrics.

c) Electrical characterization:

The high electrical resistivity of glass resulted in lower insertion loss and cross-talk between closely spaced TPVs. However, the high impedance of glass results in power-ground plane resonances in glass interposers that affected the signal and power integrity in glass interposers. Therefore, novel solutions are required to suppress such resonances and provide the highest quality signal and power delivery in 3D glass interposers.

7.4 Publications, Patent and Award

This work resulted in the following peer reviewed journal and conference publications:

Journal and Conference publications

1. 'Low-Cost Thin Glass Interposers as a Superior Alternative to Silicon and Organic Interposers for Packaging of 3-D ICs' *V. Sukumaran et al, Components, Packaging and Manufacturing Technology, IEEE Transactions, 2012.*
2. 'Design, Fabrication and Characterization of Ultra-thin 3D Glass Interposers with Through Package vias at same pitch as TSVs in Silicon' *V. Sukumaran et.al. Components, Packaging and Manufacturing Technology, IEEE Transaction, 2014*
3. 'Modeling, Design, Fabrication, and Demonstration of Band-Pass-Filters in Glass Interposer with Through-Package-Vias' *S. Sitaraman, V. Sridharan, V. Sukumaran et.al. Submitted to Components, Packaging and Manufacturing Technology, IEEE Transaction, 2013*
4. 'Ultra-miniaturized Band-Pass Filters enabled by Ultra-thin 3D IPD Glass Packages' *S. Sitaraman, V. Sukumaran, M. Raj, Y. Suzuki, S. J Kim, V. Sundaram and R R Tummala, Submitted to IEEE Micro-wave letters, 2013*

5. ‘Modeling, Design, Analysis and Characterization of 3-D Glass Interposers as an alternative to logic-to-memory bandwidth than 3D-IC stack’ *G. Kumar, V. Sukumaran, V. Sundaram, R. R. Tummala. To be submitted to IEEE CPMT, 2014*

This work resulted in the following conference proceedings:

1. ‘Ultra-miniaturized and surface-mountable Glass-Based 3D IPAC Packages for RF Modules’, *Yoichiro Sato, Vijay Sukumaran et al. Presented at ECTC 2013, Las Vegas, 2013*
2. ‘Reliability of TPVs in Glass’, *Kaya Demir, Yoichiro Sato, Koushik R, Vijay Sukumaran et al. Presented at ECTC 2013, Las Vegas, 2013*
3. ‘3D Glass Interposers: Design, Fabrication and Reliability’, *V. Sukumaran et.al Presented at Global Interposer Technology workshop, Georgia Institute of Technology, December 2011*
4. ‘Electrical Modeling, Design and Characterization of Glass Interposer with Fine-pitch Through-Package Vias’ *V. Sukumaran et al. Electronic Components and Technology Conference (ECTC), 2011, Orlando*
5. ‘High Density Electrical Feed-throughs in Advanced Biocompatible Organic Substrates for Retinal Implants’ *Venky Sundaram, Jim Weiland (USC), Vijay Sukumaran et al. Electronic Components and Technology Conference (ECTC), 2011, Orlando*
6. ‘Glass Interposer as an Alternative to 3D ICs for High Bandwidth Logic-Memory Integration’ *Gokul Kumar, Tapobrata Bandyopadhyay, Vijay Sukumaran et al. Electronic Components and Technology Conference (ECTC), 2011, Orlando*
7. 'Glass as an Electronic Package Substrate for Consumer and Biomedical Applications' *Vijay Sukumaran et al. Presented at The American Ceramic*

Society's 2010 Glass & Optical Materials Division Annual Meeting 2010 – Corning Newyork

8. 'Through-Package Via Formation and Metallization in Low Cost and Fine Pitch 3D Glass Interposers' *Vijay Sukumaran et al. Presented at the 60th Electronic Components and Technology Conference 2010, Las Vegas*
9. 'High Quality Bandpass Filter Design & Fabrication in 3D Glass interposer with Through Package Via (TPV)' *Vivek Sridharan, Sunghwan Min, Venky Sundaram, Vijay Sukumaran et al. Presented at the 60th Electronic Components and Technology Conference 2010, Las Vegas*
10. 'Trend from ICs to 3D ICs to 3D Systems' *Rao Tummala, Venky Sundaram, Ritwik Chatterjee, P. Markodeya Raj, Nitesh Kumbhat, Vijay Sukumaran et al. Presented in the IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA. September 2009. [Invited paper]*

Patent Application

- Venky Sundaram, Rao R Tummala, Vijay Sukumaran, Fuhan Liu, Vivek Sridharan, Qiao Chen, "Through-Package-Via (TPV) Structures On Inorganic Interposer And Methods For Fabricating Same," US20130119555 A1, 2013.

Award

- Intel best paper award – ECTC 2010

REFERENCES

[1] R. R. Tummala, "SOP: what is it and why? A new microsystem-integration technology paradigm-Moore's law for system integration of miniaturized convergent systems of the next decade," *Advanced Packaging, IEEE Transactions on,* vol. 27, pp. 241-249, 2004.

[2] R. R. Tummala, "Packaging: past, present and future," in *Electronic Packaging Technology, 2005 6th International Conference on*, 2005, pp. 3-7.

[3] R. R. Tummala, "Moore's law meets its match (system-on-package)," *Spectrum, IEEE,* vol. 43, pp. 44-49, 2006.

[4] C. Youngjoon, J. Hyojin, and K. Hyunbo, "Future evolution of memory subsystem in mobile applications," in *Memory Workshop (IMW), 2010 IEEE International*, 2010, pp. 1-2.

[5] D. W. Kim, R. Vidhya, B. Henderson, U. Ray, S. Gu, W. Zhao, *et al.*, "Development of 3D through silicon stack (TSS) assembly for wide IO memory to logic devices integration," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 77-80.

[6] C. C. Liu, I. Ganusov, M. Burtscher, and S. Tiwari, "Bridging the processor-memory performance gap with 3D IC technology," *Design & Test of Computers, IEEE,* vol. 22, pp. 556-564, 2005.

[7] J. Roullard, A. Farcy, S. Capraro, T. Lacrevaz, C. Bermond, G. Houzet, *et al.*, "Evaluation of 3D interconnect routing and stacking strategy to optimize high speed signal transmission for memory on logic," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 8-13.

[8] P. Leduca, F. De Crecy, M. Fayolle, B. Charlet, T. Enot, M. Zussy, *et al.*, "Challenges for 3D IC integration: bonding quality and thermal management,"

in *International Interconnect Technology Conference, IEEE 2007*, 2007, pp. 210-212.

[9] C. Meng-Fan, C. Pi-Feng, W. Wei-Cheng, C. Ching-Hao, and S. Shyh-Shyuan, "Challenges and trends in low-power 3D die-stacked IC designs using RAM, memristor logic, and resistive memory (ReRAM)," in *ASIC (ASICON), 2011 IEEE 9th International Conference on*, 2011, pp. 299-302.

[10] G. Kumar, T. Bandyopadhyay, V. Sukumaran, V. Sundaram, L. Sung-Kyu, and R. Tummala, "Ultra-high I/O density glass/silicon interposers for high bandwidth smart mobile applications," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 217-223.

[11] V. Sundaram and R. R. Tummala, "Ultra-thin interposer assembly with through vias," US Patent Application, 2012.

[12] B. Banijamali, S. Ramalingam, K. Nagarajan, and R. Chaware, "Advanced reliability study of TSV interposers and interconnects for the 28nm technology FPGA," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 285-290.

[13] B. Banijamali, S. Ramalingam, K. Namhoon, and C. Wyland, "Ceramics vs. low-CTE organic packaging of TSV silicon interposers," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 573-576.

[14] E. Klink, B. Garben, A. Huber, D. Kaller, S. Grivet-Talocia, and G. A. Katopis, "Evolution of organic chip packaging technology for high speed applications," *IEEE Transactions on Advanced Packaging*, vol. 27, pp. 4-9, 2004.

[15] B. Garben, A. Huber, D. Kaller, E. Klink, and S. Grivet-Talocia, "Organic chip packaging technology for high speed processor applications," in *6th IEEE Workshop on Signal Propagation on Interconnects, SPI, May 12, 2002 - May 15, 2002*, Pisa, Italy, 2002, pp. 119-122.

[16] R. R. Tummala, V. Sundaram, R. Chatterjee, P. Markondeya Raj, N. Kumbhat, V. Sukumaran, *et al.*, "Trend from ICs to 3D ICs to 3D systems," in *2009 IEEE Custom Integrated Circuits Conference, CICC '09, September 13, 2009 - September 16, 2009*, San Jose, CA, United states, 2009, pp. 439-444.

[17] R. R. Tummala, P. M. Raj, S. Atmur, S. Bansal, S. Banerji, F. Liu, *et al.*, "Fundamental limits of organic packages and boards and the need for novel ceramic boards for next generation electronic packaging," 2004, pp. 417-422.

[18] M. Sunohara, T. Tokunaga, T. Kurihara, and M. Higashi, "Silicon interposer with TSVs (through silicon vias) and fine multilayer wiring," in *2008 58th Electronic Components and Technology Conference, ECTC, May 27, 2008 - May 30, 2008*, Lake Buena Vista, FL, United states, 2008, pp. 847-852.

[19] R. R. T. a. V. Sundaram. (2011) Impact of 3D ICs with TSV is Profound But Complex and Costly - Is There A Better Way? *Chip Scale Review*. Available: http://www.chipscalereview.com/issues/0711/content/CSR_July-August-2011_digital.pdf

[20] S. G. et.al. Ultra-Slim Flexible Glass for Electronic Applications [Online]. Available: http://www.lehigh.edu/imi/eciworkshop/04D_Garner.pdf

[21] I. SCHOTT North America. (2014, 01/20/2014). *Ultra-Thin Glass*. Available: http://www.us.schott.com/advanced_optics/english/products/wafers-and-thin-glass/glass-wafer-and-substrates/ultra-thin-glass/index.html

[22] S. Saeki. (2012). *Asahi Glass Makes It Easy to Handle 0.1mm-thick Glass Substrate*. Available: http://techon.nikkeibp.co.jp/english/NEWS_EN/20120602/221251/

[23] K. Demir, K. Ramachandran, Y. Sato, C. Qiao, V. Sukumaran, R. Pucha, *et al.*, "Thermomechanical and electrochemical reliability of fine-pitch through-package-copper vias (TPV) in thin glass interposers and packages," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 353-359.

[24] C. Sangbeom, Y. Joshi, V. Sundaram, Y. Sato, and R. Tummala, "Comparison of thermal performance between glass and silicon interposers," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 1480-1487.

[25] Q. Xian, S. Gottschall, N. Kumbhat, P. M. Raj, K. Sungjin, V. Sundaram, *et al.*, "Large silicon, glass and low CTE organic interposers to printed wiring board SMT interconnections using copper microwire arrays," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 867-871.

[26] Y. Kanemitsu and Y. Tanaka, "Mechanism of crack formation in glass after high-power laser pulse irradiation," *Journal of Applied Physics,* vol. 62, pp. 1208-1211, 1987.

[27] P. Yun-Kwon, P. Heung-Woo, L. Duck-Jung, P. Jung-Ho, S. In-Sang, K. Chung-Woo, *et al.*, "A novel low-loss wafer-level packaging of the RF-MEMS devices," in *Micro Electro Mechanical Systems, 2002. The Fifteenth IEEE International Conference on*, 2002, pp. 681-684.

[28] L. Ju-Yong, L. Sung-Woo, L. Seung-Ki, and P. Jae-Hyoung, "Wafer level packaging for RF MEMS devices using void free copper filled through glass via," in *Micro Electro Mechanical Systems (MEMS), 2013 IEEE 26th International Conference on*, 2013, pp. 773-776.

[29] J. Y. Lee, S. K. Lee, and J. H. Park, "Fabrication of void-free copper filled through-glass-via for wafer-level RF MEMS packaging," *Electronics Letters*, vol. 48, pp. 1076-1077, 2012.

[30] M. Topper, I. Ndip, R. Erxleben, L. Brusberg, N. Nissen, H. Schroder, *et al.*, "3-D Thin film interposer based on TGV (Through Glass Vias): An alternative to Si-interposer," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 66-73.

[31] H. C. USA. Glass Circuit Board (GCB) with Photosensitive Glass [Online]. Available: http://www.hoyaoptics.com/pdf/photosensitive_glass_circuit_board.pdf

[32] S. Takahashi, K. Tatsukoshi, M. Ono, and K. Kitaoka, "TGV technology for Glass interposer," in *Electronic System-Integration Technology Conference (ESTC), 2012 4th*, 2012, pp. 1-3.

[33] T. Akashi, Y. Yoshimura, and S. Higashiyama, "Deep reactive ion etching of pyrex glass using a bonded silicon wafer as an etching mask," in *Micro Electro Mechanical Systems, 2005. MEMS 2005. 18th IEEE International Conference on*, 2005, pp. 520-523.

[34] L. Li, T. Abe, and M. Esashi, "Smooth surface glass etching by deep reactive ion etching with SF6 and Xe gases," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 21, pp. 2545-2549, 2003.

[35] X. Li, T. Abe, and M. Esashi, "Deep reactive ion etching of Pyrex glass using SF6 plasma," *Sensors and Actuators A: Physical*, vol. 87, pp. 139-145, 1/5/ 2001.

[36] L. Xinghua, T. Abe, Y. Liu, and M. Esashi, "High density electrical feedthrough fabricated by deep reactive ion etching of Pyrex glass," in *Micro Electro Mechanical Systems, 2001. MEMS 2001. The 14th IEEE International Conference on*, 2001, pp. 98-101.

[37] A. Ben-Yarkar, "Morphology of femtosecond-laser-ablated borosilicate glass surfaces " *Applied Physics Letters*, vol. 83, 2003.

[38] A. Ben-Yarkar, "Femtosecond laser ablation properties of borosilicate glass," *Journal of Applied Physics*, vol. 96, 2004.

[39] Y.-T. Chen, "Excimer laser ablation of glass-based arrayed microstructures for biomedical, mechanical, and optical applications " *Journal of Laser Applications*, vol. 17, 2005.

[40] D. Bhatt, K. Williams, D. A. Hutt, and P. P. Conway, "Process Optimisation and Characterization of Excimer Laser Drilling of Microvias in Glass," in *Electronics Packaging Technology Conference, 2007. EPTC 2007. 9th*, 2007, pp. 196-201.

[41] K. Bernd, "Drilling of glass by excimer laser mask projection technique," *Journal of Laser Applications*, vol. 12, pp. 189-193, 2000.

[42] A. A. Tseng, Y.-T. Chen, and K.J. Ma, "Fabrication of high-aspect-ratio microstructures using excimer laser," *Optics and Lasers in Engineering*, vol. 41, pp. 827-847, 6// 2004.

[43] L. Brusberg, M. Queisser, C. Gentsch, H. Schröder, and K.-D. Lang, "Advances in CO2-Laser Drilling of Glass Substrates," *Physics Procedia,* vol. 39, pp. 548-555, // 2012.

[44] C. K. Chung, H. C. Chang, T. R. Shih, S. L. Lin, E. J. Hsiao, Y. S. Chen, *et al.*, "Water-assisted CO2 laser ablated glass and modified thermal bonding for capillary-driven bio-fluidic application," *Biomedical Microdevices,* vol. 12, pp. 107-114, 2010/02/01 2010.

[45] S. Yu, Y. Daquan, H. Ran, D. Fengwei, S. Xiaofeng, and W. Lixi, "The development of low cost Through Glass Via (TGV) interposer using additive method for via filling," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2012 13th International Conference on*, 2012, pp. 49-51.

[46] C. K. Chung, S. L. Lin, H. Y. Wang, T. K. Tan, K. Z. Tu, and H. F. Lung, "Fabrication and simulation of glass micromachining using CO2 laser processing with PDMS protection," *Applied Physics A,* vol. 113, pp. 501-507, 2013/11/01 2013.

[47] M. Electric. Mitsubishi Electric Develops Micro Glass-processing Technology Incorporating Pulsed CO_2 Laser [Online]. Available: http://www.mitsubishielectric.com/news/2014/0213-c.html

[48] O. Nukaga, T. Shioiri, S. Yamamoto, and T. Suemasu, "Glass interposer with high-density three-dimensional structured TGV for 3D system integration," in *3D Systems Integration Conference (3DIC), 2013 IEEE International*, 2013, pp. 1-4.

[49] W. Bor Kai, C. Yi-An, A. Shorey, and G. Piech, "Thin glass substrates development and integration for through glass vias (TGV) with copper (Cu)

interconnects," in *Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2012 7th International*, 2012, pp. 247-250.

[50] Cornejo, "Method for making Glass Inteposer panels," 8,584,354 B2, 2013.

[51] R. P. Ralph Delmdahl, Rolf Senczuk, Jan Brune, "High Density Through Glass Vias for Advanced Chip Packaging," presented at the ICALEO, Miami, FL, 2013.

[52] S. Garner. Ultra-slim Flexible Glass Substrates for Display Applications [Online]. Available: www.corning.com/WorkArea/downloadasset.aspx?id=50407

[53] G. S. Glaesemann. The Sterngth of Thin Flexible Glass Sheets [Online]. Available: www.corning.com/WorkArea/downloadasset.aspx?id=51177

[54] S. Yoshida. AGC's Carrier Glass Technology Enables Current Production Processes to Hanlde Ultra-thin Glass [Online]. Available: http://www.agc.com/english/news/2012/0530e.pdf

[55] G. R. Trott, "Glass Wafer Mechanical Properties: A Comparison to Silicon," A. Shorey, Ed., ed.

[56] D. A. Tammaro. Substartes for Flexible AM Displays [Online]. Available: www.corning.com/WorkArea/downloadasset.aspx?id=52637

[57] S. W. C. Mei Wen, "Strengthening Glass by Polymeric Coatings," in *International Coating science and Technology Symposium*, Marina Del Ray, California, 2008.

[58] S. I. Sil'vestrovich, M. I. Stolyarov, L. M. Gurikova, G. V. Stolyarova, E. A. Shcheredina, and O. N. Koshelkina, "Protective effect of polymer coatings on glass surfaces," *Glass and Ceramics*, vol. 29, pp. 718-722, 1972/11/01 1972.

[59] A. Weber, S. Deutschbein, A. Plichta, and A. Habeck, "6.3: Thin Glass-Polymer Systems as Flexible Substrates for Displays," *SID Symposium Digest of Technical Papers*, vol. 33, pp. 53-55, 2002.

[60] Y. J. Lin, C. C. Hsieh, C. H. Yu, C. H. Tung, and D. C. H. Yu, "Study of the thermo-mechanical behavior of glass interposer for flip chip packaging applications," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 634-638.

[61] J. E. Ritter, W. Gu, and T. J. Lardner, "Effectiveness of polymer coatings on reducing indention damage in glass," *Polymer Engineering & Science*, vol. 32, pp. 1372-1378, 1992.

[62] J. E. Ritter, D. R. Sioui, and T. J. Lardner, "Indentation behavior of polymer coatings on glass," *Polymer Engineering & Science*, vol. 32, pp. 1366-1371, 1992.

[63] D. A. Hutt, K. Williams, P. P. Conway, F. M. Khoshnaw, C. Xiaoyun, and B. Deepa, "Challenges in the Manufacture of Glass Substrates for Electrical and Optical Interconnect," in *Electronics Systemintegration Technology Conference, 2006. 1st*, 2006, pp. 1279-1285.

[64] Y. Chen, E. T. Kang, K. G. Neoh, and W. Huang, "Electroless Metallization of Glass Surfaces Functionalized by Silanization and Graft Polymerization of Aniline," *Langmuir*, vol. 17, pp. 7425-7432, 2001/11/01 2001.

[65] C. Xiaoyun, D. A. Hutt, and P. P. Conway, "An investigation of electroless copper films deposited on glass," in *Electronics System-Integration Technology Conference, 2008. ESTC 2008. 2nd*, 2008, pp. 105-110.

[66] C. Xiaoyun, D. Bhatt, D. A. Hutt, K. Williams, and P. P. Conway, "Copper Deposition and Patterning for Glass Substrate Manufacture," in *Electronics Packaging Technology Conference, 2007. EPTC 2007. 9th*, 2007, pp. 37-42.

[67] H. Baofeng, D. P. Webb, J. Petzing, and R. Leach, "Improving plated copper adhesion for metallisation of glass PCBs," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*, 2011, pp. 1-5.

[68] K. Sugioka, T. Hongo, H. Takai, and K. Midorikawa, "Selective metallization of internal walls of hollow structures inside glass using femtosecond laser," *Applied Physics Letters*, vol. 86, pp. 171910-171910-3, 2005.

[69] J. Xu, Y. Liao, H. Zeng, Y. Cheng, Z. Xu, K. Sugioka, *et al.*, "Mechanism study of femtosecond laser induced selective metallization (FLISM) on glass surfaces," *Optics Communications*, vol. 281, pp. 3505-3509, 2008.

[70] E. Delamarche, M. Geissler, J. Vichiconti, W. S. Graham, P. A. Andry, J. C. Flake, *et al.*, "Electroless Deposition of NiB on 15 Inch Glass Substrates for the Fabrication of Transistor Gates for Liquid Crystal Displays," *Langmuir*, vol. 19, pp. 5923-5935, 2003/07/01 2003.

[71] E. Delamarche, J. Vichiconti, S. A. Hall, M. Geissler, W. Graham, B. Michel, *et al.*, "Electroless Deposition of Cu on Glass and Patterning with Microcontact Printing," *Langmuir*, vol. 19, pp. 6567-6569, 2003/08/01 2003.

[72] R. B. S. Bamberg, J. Etzkorn, F. Brüning, "Novel Wet Chemical Copper Metallization for Glass Interposers," presented at the IMAPS 8th International Conference and Exhibition on Device Packaging, Scottsdale/Fountain Hills, Arizona USA, 2011.

[73] C. Le, W. Qian, C. Jian, M. Guangrui, H. Yang, and L. Taekoo, "Study of glass metallization and adhesion evaluation for TGV application," in *Electronic Packaging Technology (ICEPT), 2013 14th International Conference on*, 2013, pp. 217-220.

[74] P. Ogutu, E. Fey, P. Borgesen, and N. Dimitrov, "Hybrid Method for Metallization of Glass Interposers," *Journal of The Electrochemical Society,* vol. 160, pp. D3228-D3236, January 1, 2013 2013.

[75] S. Takahashi, K. Horiuchi, K. Tatsukoshi, M. Ono, N. Imajo, and T. Mobely, "Development of Through Glass Via (TGV) formation technology using electrical discharging for 2.5/3D integrated packaging," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 348-352.

[76] T. M. Technologies. How Triton TGV Interposers are made... [Online]. Available: http://www.tritonmicrotech.com/triton-micro-technology

[77] D. A. Hutt, K. Williams, P. P. Conway, F. M. Khoshnaw, C. Xiaoyun, and D. Bhatt, "Challenges in the Manufacture of Glass Substrates for Electrical and Optical Interconnect," in *Electronics Systemintegration Technology Conference, 2006. 1st*, 2006, pp. 1279-1285.

[78] C. Xiaoyun, D. Bhatt, F. Khoshnaw, D. A. Hutt, and P. P. Conway, "Glass as a Substrate for High Density Electrical Interconnect," in *Electronics Packaging Technology Conference, 2008. EPTC 2008. 10th*, 2008, pp. 12-17.

[79] F. M. Khoshnaw, L. P. P. Conway, D. A. Hutt, and K. Williams, "Glass Multilayer Lamination for PCB Manufacture using Pressure Assisted Low Temperature Bonding," in *Electronics Packaging Technology Conference, 2007. EPTC 2007. 9th*, 2007, pp. 504-509.

[80] L. Brusberg, N. Schlepple, and H. Schroder, "Chip-to-chip communication by optical routing inside a thin glass substrate," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 805-812.

[81] L. Brusberg, H. Schroder, M. Topper, and H. Reichl, "Photonic System-in-Package technologies using thin glass substrates," in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 930-935.

[82] H. Schroder, L. Brusberg, R. Erxleben, I. Ndip, M. Topper, N. F. Nissen, *et al.*, "glassPack: A 3D glass based interposer concept for SiP with integrated optical interconnects," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1647-1652.

[83] L. Ching-Kuan, C. Chun-Hsien, C. Chia-Wen, S. Wen-Wei, F. Huan-Chun, L. Yuan-Chang, *et al.*, "Investigation of the process for glass interposer," in *Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2013 8th International*, 2013, pp. 194-197.

[84] C. Chun-Hsien, Y. Hsun, L. Ching-Kuan, L. Yu-Min, C. Ren-shin, Z. Chau-Jie, *et al.*, "Performance and process characteristic of glass interposer with through-glass-via(TGV)," in *3D Systems Integration Conference (3DIC), 2013 IEEE International*, 2013, pp. 1-7.

[85] B. Moyer. (2014, 2/18/2014). Glass Interposers: Is Thin In? *Electronic Engineering Journal*. Available: http://www.eejournal.com/archives/articles/20140106-interposers/

[86] W. C. Lai, H. H. Chuang, C. H. Tsai, E. H. Yeh, C. H. Lin, T. H. Peng, *et al.*, "300mm size ultra-thin glass interposer technology and high-Q embedded helical inductor (EHI) for mobile application," in *Electron Devices Meeting (IEDM), 2013 IEEE International*, 2013, pp. 13.4.1-13.4.4.

[87] Z. Jing, S. Xiaofeng, G. Daniel, Y. Daquan, C. Liqiang, and W. Lixi, "Modeling and finite-element full-wave simulation of glass interposer with TGVs (through-glass-vias) for 3D packaging," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*, 2011, pp. 1-4.

[88] S. Yu, Y. Daquan, Y. Shuangshou, S. Xiaofeng, Z. Jing, W. Xiuzhen, *et al.*, "Development of through glass tungsten via interconnect for 3D MEMS packaging," in *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*, 2011, pp. 774-776.

[89] T. Bandyopadhyay, "MODELING, DESIGN, AND CHARACTERIZATION OF THROUGH VIAS IN SILICON AND GLASS INTERPOSERS," PhD, Electrical and Computer Engineering, Georgia Institute of Technology, 2011.

[90] V. Sridharan, S. Min, V. Sundaram, V. Sukumaran, S. Hwang, H. Chan, *et al.*, "Design and fabrication of bandpass filters in glass interposer with through-package-vias (TPV)," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 530-535.

[91] S. Xiaofeng, S. Yu, Z. Jing, Y. Daquan, and W. Lixi, "Design of RF MEMS phase shifter packaging based on through glass via (TGV) interposer," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2012 13th International Conference on*, 2012, pp. 808-810.

[92] K. Cheolbok and Y. Yong-Kyu, "High frequency characterization and analytical modeling of through glass via (TGV) for 3D thin-film interposer and MEMS packaging," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 1385-1391.

[93] X. Biancun and M. Swaminathan, "Modeling and analysis of SSN in silicon and glass interposers for 3D systems," in *Electrical Performance of Electronic Packaging and Systems (EPEPS), 2012 IEEE 21st Conference on*, 2012, pp. 268-271.

[94] F. Liu, Venky Sundaram, Rao R Tummala, Vijay Sukumaran, Vivek Sridharan, Qiao Chen, "Through-Package-Via (TPV) Structures On Inorganic Interposer And Methods For Fabricating Same," US20130119555 A1, 2013.

[95] A. H. D. Hulsenberg, A. Bismarck, *Microstructuring of Glasses*: Springer, 2008.

[96] C. Iliescu and F. E. H. Tay, "Wet etching of glass," in *Semiconductor Conference, 2005. CAS 2005 Proceedings. 2005 International*, 2005, pp. 35-44 vol. 1.

[97] R. Cook. Via Formation in Photo-structurable Glasses [Online]. Available: http://www.3dglasssolutions.com/media/uploads/files/111115_3DGS_GT_Interposer_Workshop_Presentation_Roger_Cook.pdf

[98] K. D. a. P. Shi, "Subsurface precision machining of glass substrates by innovative lasers," 2003.

[99] J. C. Ion, *Laser Processing of Engineering Materials*: Elsevier, 2005.

[100] L. Jiang and H. Tsai, "Femtosecond laser ablation: challenges and opportunities," in *Proceeding of NSF Workshop on Research Needs in Thermal, Aspects of Material Removal, Stillwater, OK*, 2003, pp. 163-177.

[101] Coherent. Practical Considerations in the Design of Visible and UV Laser Based Micromachining Systems [Online]. Available: https://www.coherent.com/download/7771/Considerations-in-the-Design-of-Visible-UV-Laser-Based-Micromachining-Systems.pdf

[102] D. R. R. Uhlmann, & Kreidl, N. J., *Glass--science and technology*: New York: Academic Press, 1980.

[103] J. Teisseire, D. Dalmas, S. Lohou, C. Silva, and E. Barthel, "Glass strengthening by polymeric coatings: combined effect of mechanical properties and confinement," *International Journal of Fracture*, vol. 170, pp. 115-121, 2011/08/01 2011.

[104] M.-F. Chen and Y.-P. Chen, "The new technology of the materials process: microvia formation by CO2 laser drilling machine," 2005, pp. 522-527.

[105] V. Sukumaran, T. Bandyopadhyay, Q. Chen, N. Kumbhat, L. Fuhan, R. Pucha, *et al.*, "Design, fabrication and characterization of low-cost glass interposers with fine-pitch through-package-vias," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 583-588.

[106] S. Bamberg, "Improvement of Plated Copper Adhesion in Glass Interposer Applications," presented at the IMAPS, 2012.

[107] J. Xu, Y. Liao, H. Zeng, Z. Zhou, H. Sun, J. Song, *et al.*, "Selective metallization on insulator surfaces with femtosecond laser pulses," *Optics Express*, vol. 15, pp. 12743-12748, 2007.

[108] X. Cui, D. Bhatt, D. A. Hutt, K. Williams, and P. P. Conway, "Copper deposition and patterning for glass substrate manufacture," in *9th Electronics Packaging Technology Conference, EPTC 2007, December 12, 2007 - December 12, 2007*, Singapore, 2007, pp. 37-42.

[109] A. C. Kundu, M. Megahed, and D. Schmidt, "Comparison and analysis of integrated passive device technologies for wireless radio frequency module," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, 2008, pp. 683-687.

[110] W. Chen-Chao, Y. Hsueh-An, S. Ying-Chieh, L. Meng-Hsun, C. Chi-Tsung, W. Sung-Mao, *et al.*, "Analysis of high performance RF integrated passive circuits using the glass substrate," in *VLSI Packaging Workshop of Japan, 2008. VPWJ 2008. IEEE 9th*, 2008, pp. 135-138.

[111] Y. Sato, S. Sitaraman, V. Sukumaran, B. Chou, M. Junki, M. Ono, *et al.*, "Ultra-miniaturized and surface-mountable glass-based 3D IPAC packages for RF modules," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 1656-1661.

[112] B. C. Yoichiro Sato, Vijay Sukumaran, Junki Min, Motoshi Ono, Choukri Karoui, Franck Dosseul, Christian Nopper, Madhavan Swaminathan, Venky Sundaram and Rao Tummala "RF Device Integration on Glass Interposer toward 3D-IPAC Packages," presented at the IMAPS Device packaging, Orlando, 2013.